MALT-PCIe

IP-Core. PCIe analog physical layer

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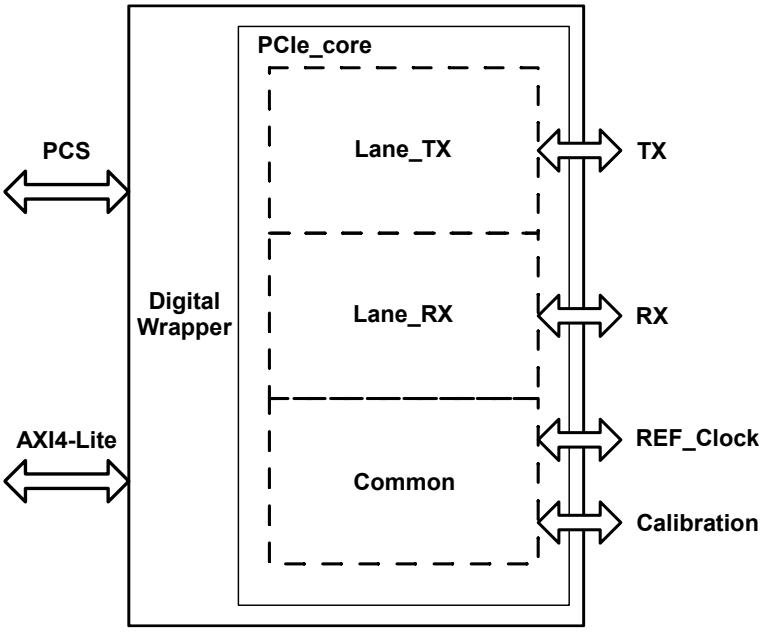

The IP-core is designed to implement functions in accordance with «PCI Express Base Specification 4.0», ensuring backward compatibility with PCIe 1, 2, and 3. Data serialization and transmission, as well as channel adaptation, reception, and deserialization, are performed at speeds of up to 16 Gbps over an x8 data bus. The IP-core detects the presence of a receiver at the other end of the line, as well as a low-frequency signal at the receiver input. Generation of clock signals required for operation of the receiving and transmitting components, as well as calibration of the transmitter output impedance and the receiver input impedance at DC, are implemented directly in the IP-core. Diagnostics and debugging are performed via the JTAG interface according to the IEEE 1149.1 standard. The self-configuring architecture requires no training templates or user configuration. The solution is focused on applications in processors and SoCs for telecommunications equipment, in storage devices, in network switches and routers, in accelerators, GPUs and tensor chips for high-performance computing.

Technical specifications

IP-Core type:	Physical (HARD IP)
IP-Core status:	In development
Technology, nm:	28
Packaging method, -:	Flip Chip support
Backward compatibility, -:	PCIe 1, 2 & 3
Link performance (x1), GB/s:	2
Link performance (x1), GT/s:	16
Encoding, -:	128b/130b
Data Bus, bits:	32
Configuration of data bus lines, -:	up to x8
Supply voltage, V:	0.9 & 1.8
Power dissipation, mW:	800
Macro area, mm^2:	2.1
Delivery terms:	Preparation for delivery is required

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Applications

- Processors and SoCs for telecommunication equipment;
- Storage drives and data storage systems;

- Connecting network interface drives, graphics cards, processors, and other components in server platforms;
- Network switches, routers, data transmission systems, and Ethernet-related applications;
- Accelerators, GPUs, and Tensor Chips for High-Performance Computing.

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