KeyASIC

Libraries and Design IPs

March 2019

Moscow

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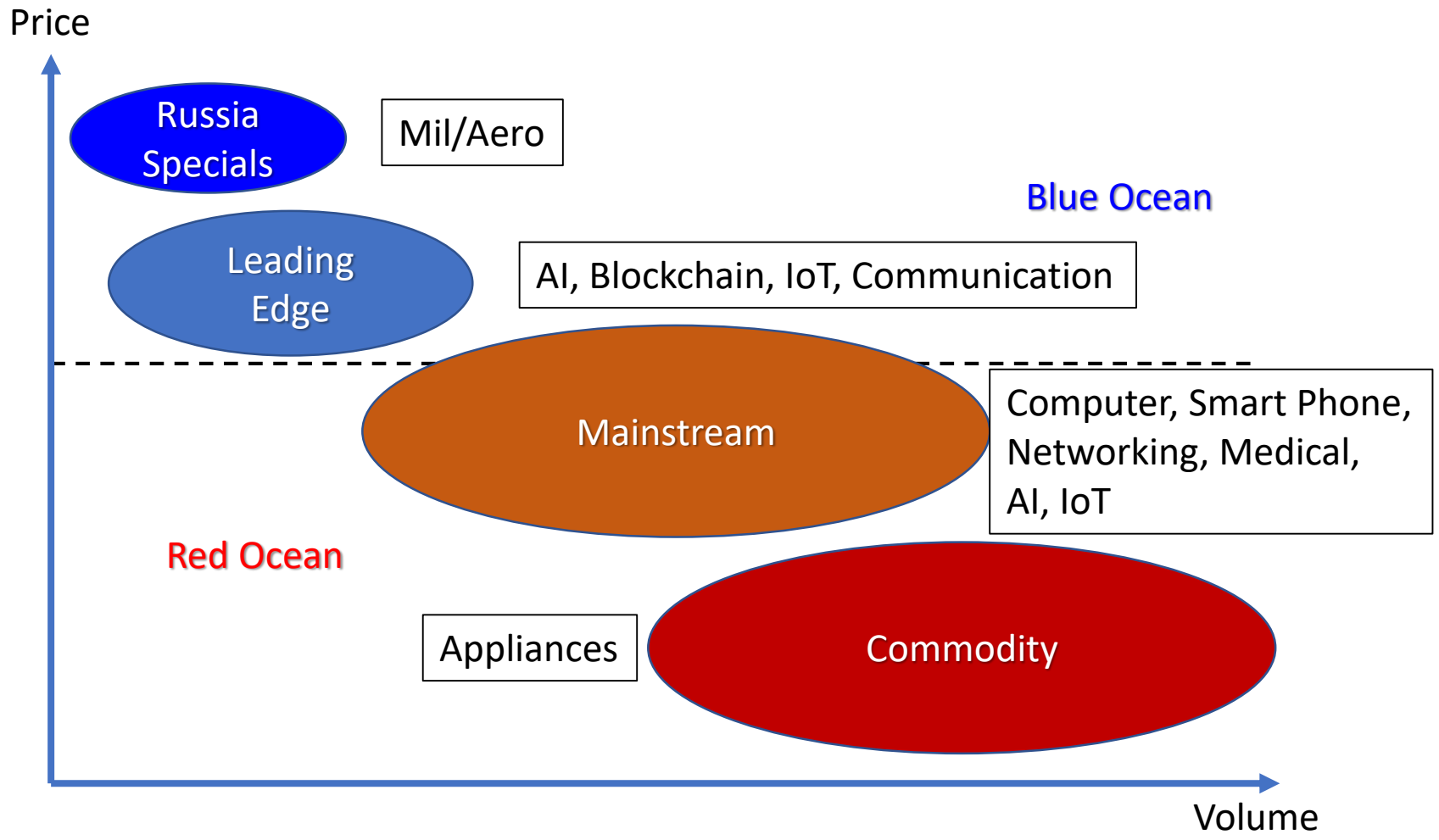
Product Position



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Design Flow

Library Definition
- Cell Architecture
- Cell Mix
- Drive Strength

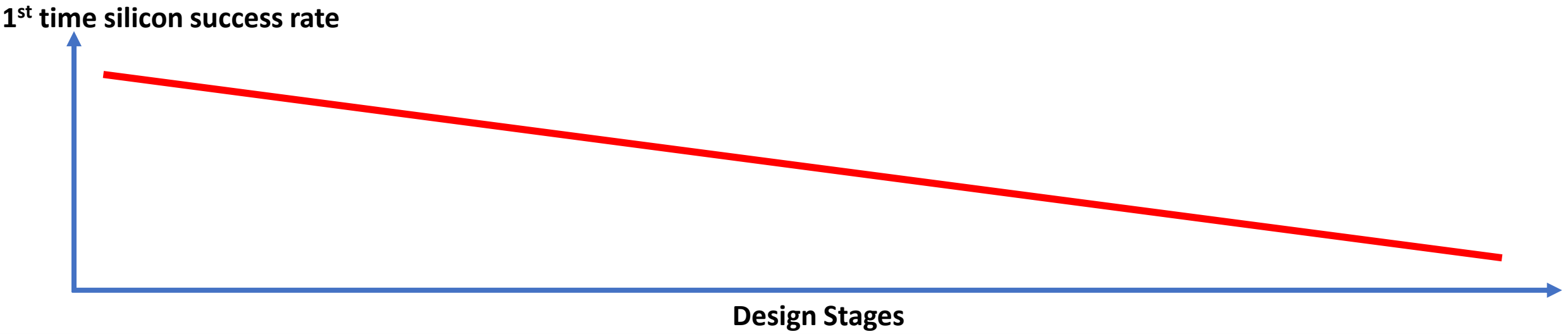
Circuit Synthesis
- Logic Restructuring
- Circuit Optimization

Topology Creation
- Circuit Re-ordering
- Transistor Placement

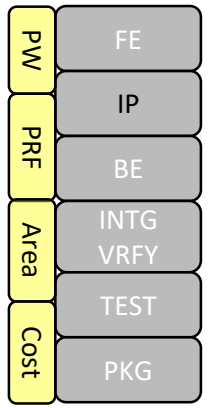
Layout Creation
- Strategy Compaction

Verification
- DRC, LVS
- Parasitic Extraction

Characteriza-tion
- .lib, LEF, GDSII, CDL
- Verilog



Strategy of Libraries & IP selection



- Readily Available IPs
  - It can help kick start the chip design and lead to shorter design cycles.
- Cheaper Price
  - Applying generic foundation IP will often be cheaper as compared to the costs associated with internal IP development, verification and (test-chip) characterization.
- Silicon Proven
  - Mature production proven IPs reduce risk.
- Quality (PPAC)
  - Select the IPs that fit your requirements in term of Power, Performance, Area and Cost.

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Case Study #1 – Analog Block

Spec	IX XXXX ADC	GXXX ADC	KA ADC
Process	Silterra 0.13um	GSMC 0.13um	Silterra 0.13um
VDD	3.3V / 1.2V	5.0V / 1.5V	3.3V / 1.2V
Conversation Rate	2MSPS	1MSPS	2MSPS
Bits	12	12	14
Area	0.31mm^2	0.32mm^2	0.28mm^2
Power	3.6mW @ 1MSPS	5mW @ 1MSPS	0.8mW w/o buffer @ 2MSPS 2.0mW w/ buffer @ 2MSPS 0.5mW w/o buffer @ 1MSPS 1.8mW w/ buffer @ 1MSPS
Input range Input mode	N/A	1.8V ~ 5.5V	2.7V ~ 3.6V
Temperature	-40°C ~ 85°C	-40°C ~ 85°C	-40°C ~ 125°C
Channel	16 (single-mode) 8 (diff-mode)	16 (single-mode)	16 (single-mode) 8 (diff-mode)
Input load	30pF	26pF	13pF (single-mode) 26pF (diff-mode)

PW
FE
IP
PRF
BE
Area
INTG
VRFY
TEST
Cost
PKG

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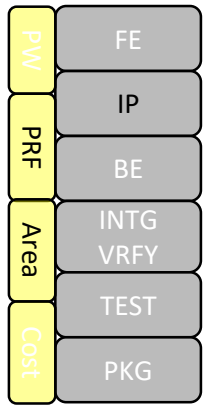
Case Study #2 – Fundamental IP



Spec Features	SXXXX GPIO#1	KA GPIO#1
Process Technology	Silterra C13G	Silterra C13G
I/O Standard	LVCMOS	LVCMOS
Bonding	Staggered	Inline
Size	Big (0.0141area^2)	Small (0.0065area^2)
ESD / LU Compliant	Yes	Yes
Special design: Power-on-control for crowbar current	No	Yes
Pass Issues: latch-up @ high	Yes	No
Pass Issues: ESD Failure	Yes	No

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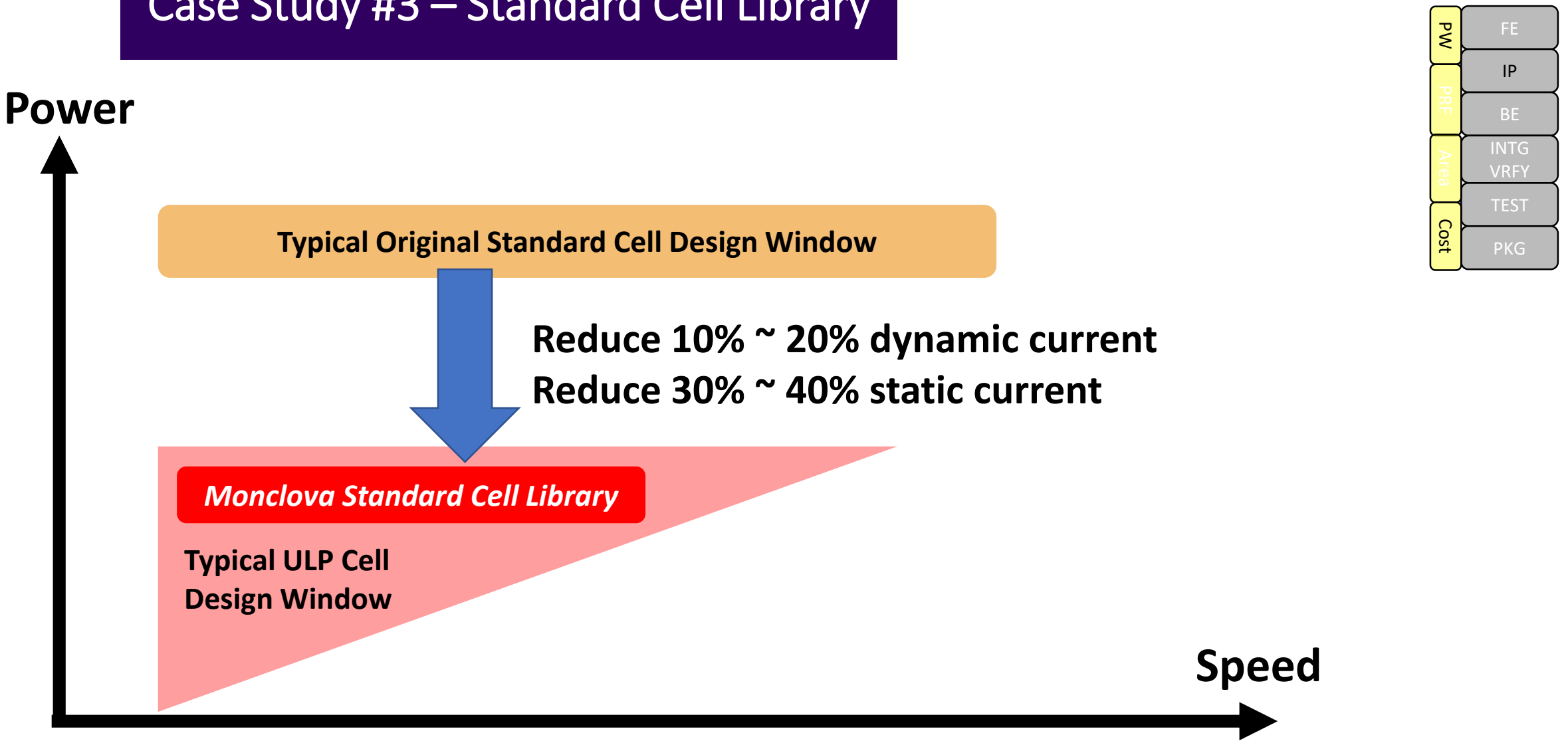
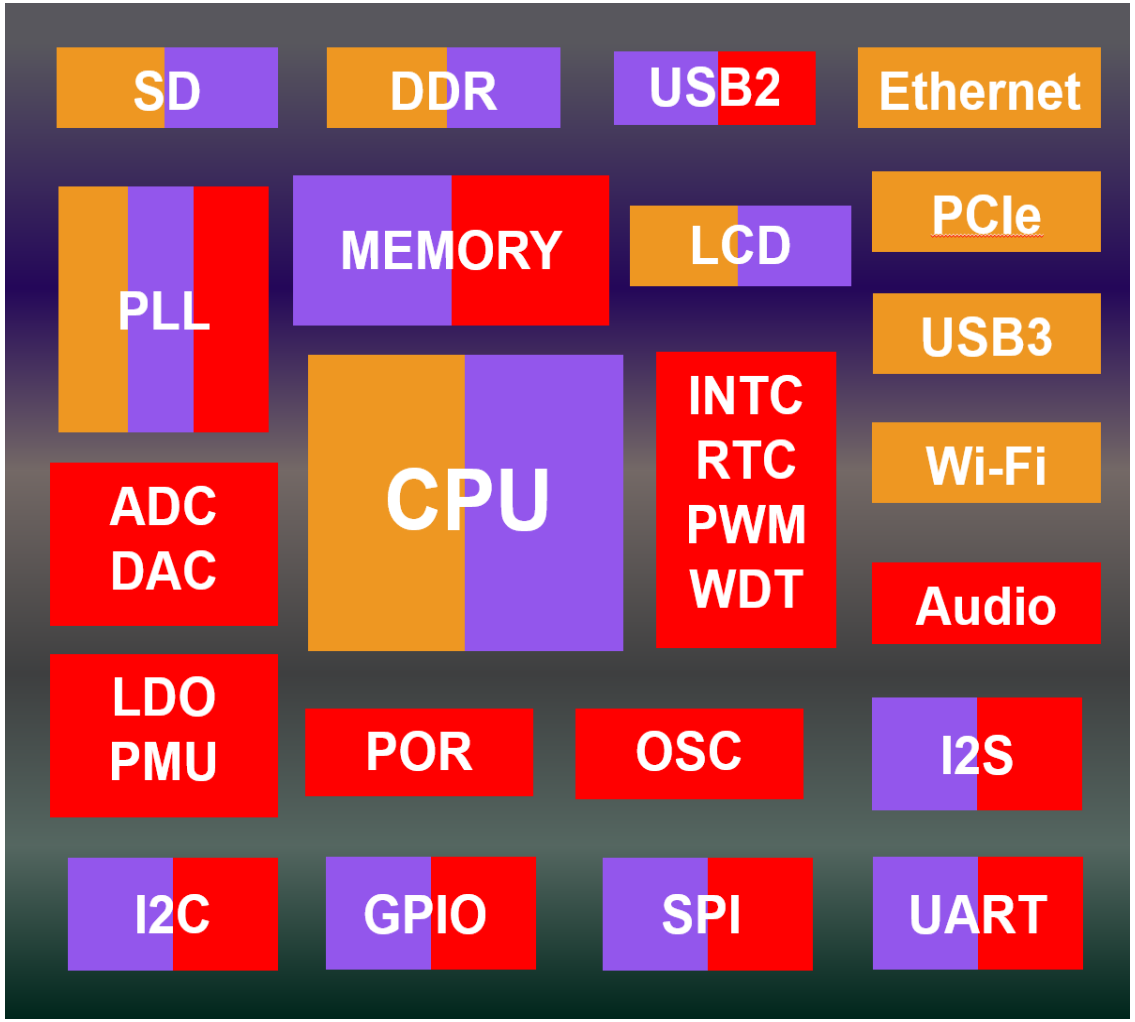
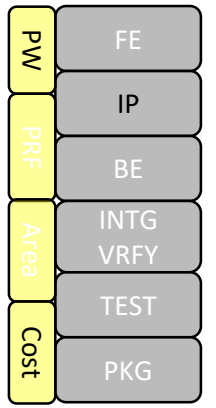
Case Study #3 – Standard Cell Library



Case Study #3 – Standard Cell Library

- Can mixed with others same process library



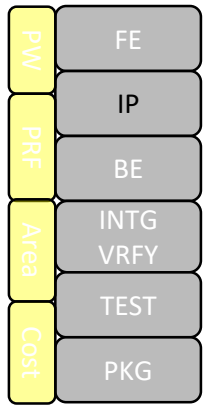


Original Library Only

Combined original & Monclova

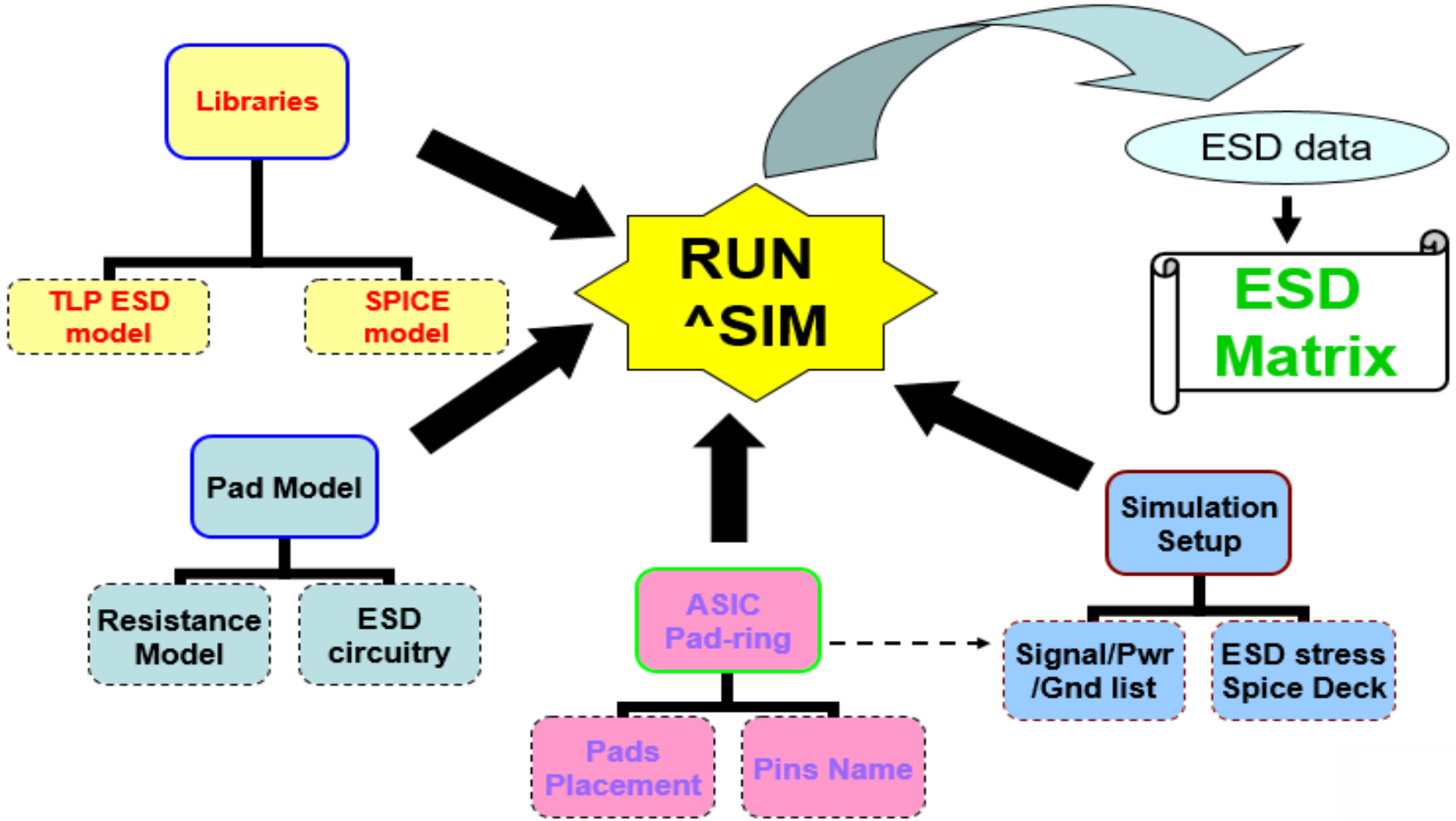
Monclova Library Only

ESD / LU Design Challenges



- No specific EDA tool for ESD simulation
- Full Chip Pad Ring simulation take times to complete

Case Study 4 - ^Sim



PW: FE, IP
PRF: BE
Area: INTG VRFY, TEST
Cost: PKG

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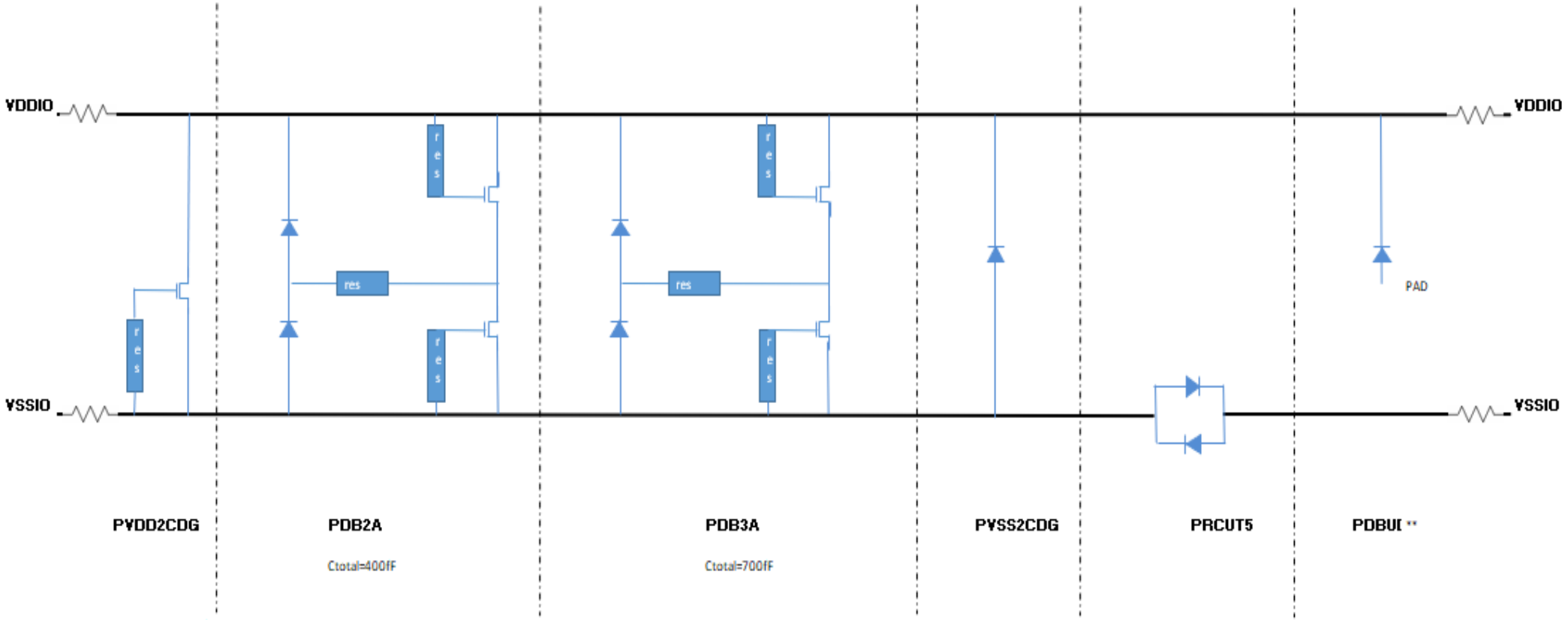
I/O Pad Modelling

PW
PRF
Area
Cost

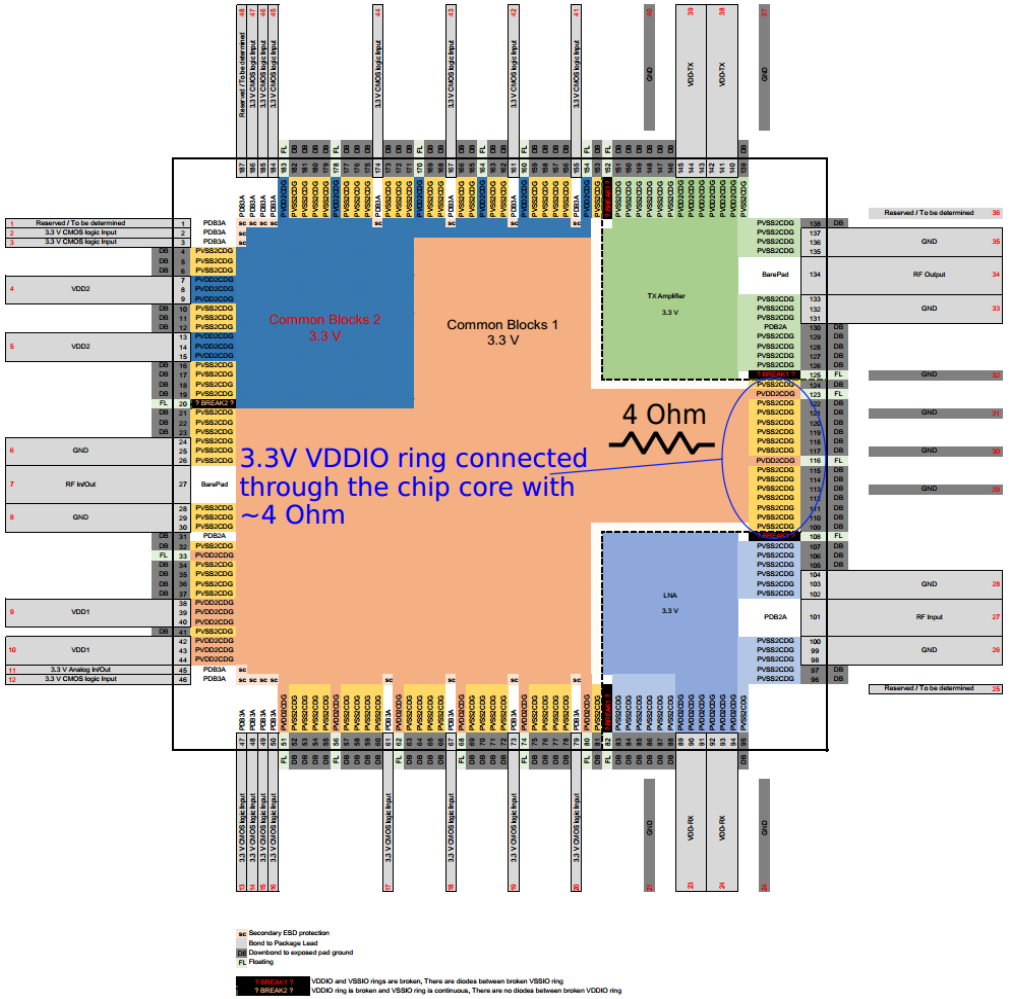
- FE
- IP
- BE
- INTG VRFY
- TEST
- PKG



* Proposed customize cells for UMIC
* POWER and GND Breakers cells will at 82, 108, 125, 152. (refer to SIRIUS_KeyAsicPADRing_07032018_v1_ea.pdf)
* Both side of PDB2A / PDB3A will have PRCUT5

** new added cell based on customer requested

Pad Ring Modelling

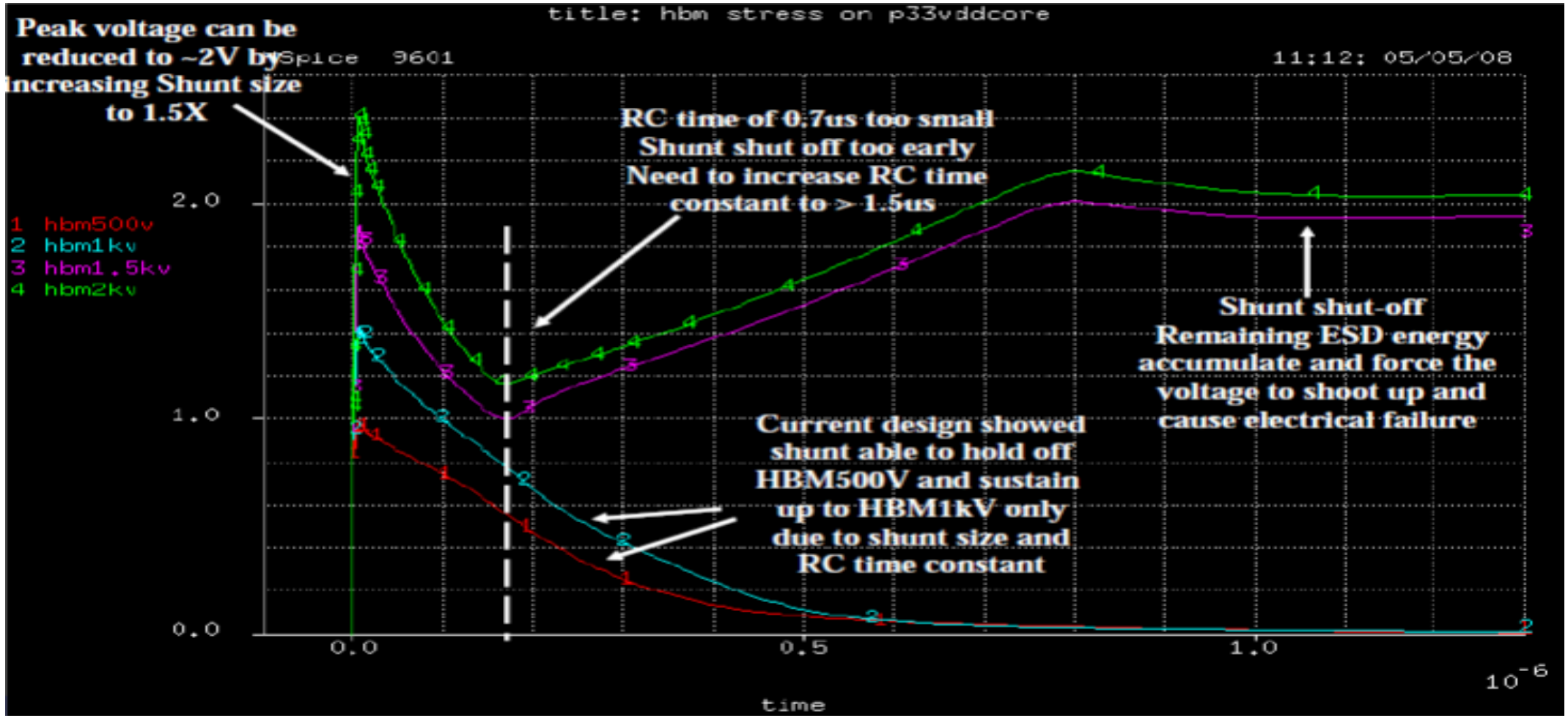


Pad#	Instance-Name	Cell-name	Side	Type	Loading	Notre
1		PDB3A	L	AI		
2		PDB3A	L	AI		
3		PDB3A	L	AI		
4		PVSS2CDG	L	power		
5		PVSS2CDG	L	power		
6		PVSS2CDG	L	power		
7		PVDD2CDG	L	power		
8		PVDD2CDG	L	power		
9		PVDD2CDG	L	power		
10		PVSS2CDG	L	power		
11		PVSS2CDG	L	power		
12		PVSS2CDG	L	power		
13		PVDD2CDG	L	power		
14		PVDD2CDG	L	power		
15		PVDD2CDG	L	power		
16		PVSS2CDG	L	power		
17		PVSS2CDG	L	power		
18		PVSS2CDG	L	power		
19		PVSS2CDG	L	power		
20		PRCUT3	L			cut only power bus
21		PVSS2CDG	L	power		
22		PVSS2CDG	L	power		
23		PVSS2CDG	L	power		
24		PVSS2CDG	L	power		
25		PVSS2CDG	L	power		
26		PVSS2CDG	L	power		
27		BarePad	L	AI		no esd? Current library have no barepad cell. ; 20-Mar: will use PDBUD
28		PVSS2CDG	L	power		
29		PVSS2CDG	L	power		
30		PVSS2CDG	L	power		
31		PDB2A	L			Cant use with this setting; 22-Mar : PAD core port will used, refer to sheet proposal
32		PVSS2CDG	L	power		
33		PVDD2CDG	L	power		
34		PVSS2CDG	L	power		
35		PVSS2CDG	L	power		
36		PVSS2CDG	L	power		
37		PVSS2CDG	L	power		
38		PVDD2CDG	L	power		
39		PVDD2CDG	L	power		

PW PRF Area Cost

FE
IP
BE
INTG VRFY
TEST
PKG

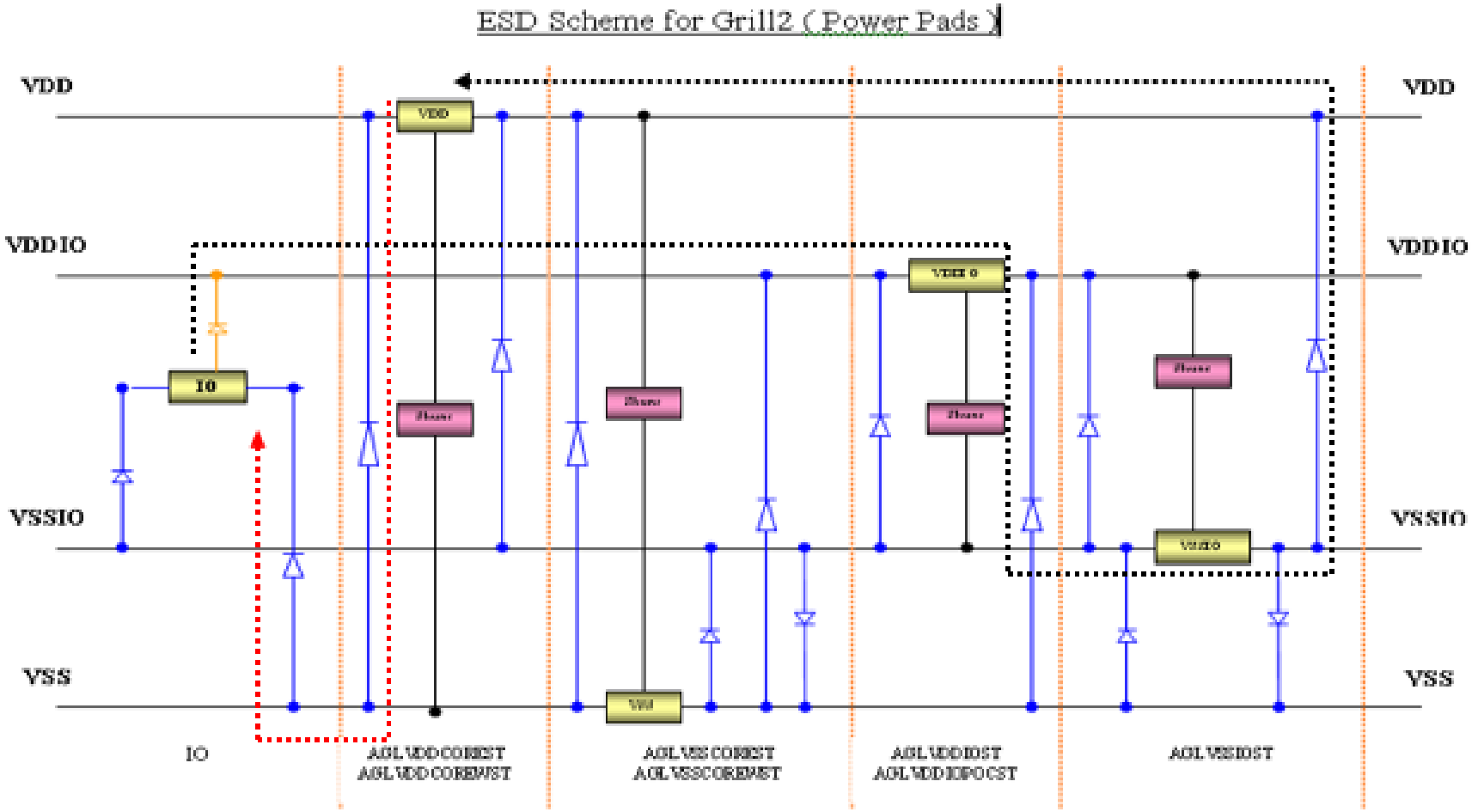
^Sim Simulation



PW
PRF
Area
Cost

FE
IP
BE
INTG VRFY
TEST
PKG

Analysis



PW: FE, IP
PRF: BE
Area: INTG VRFY
Cost: TEST, PKG

Pins(+) Pins(-)	One IO
VDD	4.977
	-1.723

Zapping Voltage : 2kV HBM model

8V IO-shunt(5V) + 2 diode(2V) + IR drop(1V)

4V Core-shunt(2V) + 1 diode(1V) + IR drop(1V)

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ESD Matrix

PW | PRF | Area | Cost

FE | IP | BE | INTG VRFY | TEST | PKG

BROOM2 ESD MATRIX — 1st March Ying Poh

Zapping Voltage : 2kV HBM model

	other IO	VDD	VSS	VDDIO	VSSIO	VDDIO DDR	VSSIO DDR	VDDIO USBD	VSSIO USBD	XVDD OSC	VSSIO OSC	VDD PLL	VDDA PLL	VSSA PLL	
VDD	7.977														VDD
	-1.723														
VSS	7.464	0.826													VSS
	-1.106	-0.729													
VDDIO	8.42	1.579	1.132												VDDIO
	-2.763	-2.271	-1.951												
VSSIO	8.371	1.539	1.084	2.663											VSSIO
	-1.951	-1.35	-1.09	-0.731											
VDDIO	8.691	2.016	1.84	3.482	2.165										VDDIO
DDR	-3.354	-2.836	-2.684	-3.166	-3.158										DDR
VSSIO	8.666	1.995	1.818	3.462	2.147	2.72									VSSIO
DDR	-2.346	-1.858	-1.675	-2.159	-2.151	-0.746									DDR
VDDIO	9.313	2.296	2.135	4.452	2.596	4.02	2.539								VDDIO
USBD	-6.767	-6.038	-5.88	-6.558	-6.511	-6.425	-6.399								USBD
VSSIO	9.283	2.267	2.105	4.418	2.561	3.983	2.502	3.969							VSSIO
USBD	-2.993	-2.271	-2.116	-2.791	-2.744	-2.655	-2.629	-0.767							USBD
XVDD	9.244	2.296	2.086	4.435	2.587	4.049	2.559	5.288	1.58						XVDD
OSC	-7.803	-7.075	-6.919	-7.599	-7.553	-7.48	-7.453	-6.272	-6.336						OSC
VSSIO	9.086	2.155	1.939	4.299	2.453	3.937	2.44	5.282	1.574	6.253					VSSIO
OSC	-2.778	-2.094	-1.927	-2.601	-2.564	-2.542	-2.517	-1.529	-1.591	-0.87					OSC
VDD	9.304	2.294	2.08	4.442	2.601	4.121	2.616	5.768	2.056	6.748	1.4				VDD
PLL	-3.692	-2.984	-2.984	-3.508	-3.47	-3.458	-3.432	-2.647	-2.703	-2.633	-2.364				PLL
VDDA	9.236	2.269	2.057	4.415	2.572	4.075	2.575	5.595	1.884	6.571	1.265	2.245			VDDA
PLL	-6.039	-5.325	-5.173	-5.849	-5.806	-5.779	-2.753	-4.856	-4.913	-4.846	-4.618	-4.622			PLL
VSSA	9.435	2.437	2.282	4.607	2.758	4.234	2.74	5.733	2.022	6.71	1.749	2.336	4.729		VSSA
PLL	-2.742	-1.998	-1.998	-2.551	-2.509	-2.491	-2.465	-1.858	-1.906	-1.858	-1.64	-1.609	-1.465		PLL
	other IO	VDD	VSS	VDDIO	VSSIO	VDDIO DDR	VSSIO DDR	VDDIO USBD	VSSIO USBD	XVDD OSC	VSSIO OSC	VDD PLL	VDDA PLL	VSSA PLL	

Summary

- Always consider about reducing Power consumption, Better Performance, Minimize Area and Cheaper Cost during the early stage of design

- Robust ESD design is a MUST

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Thank you

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Appendix

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Our IPs Portfolio

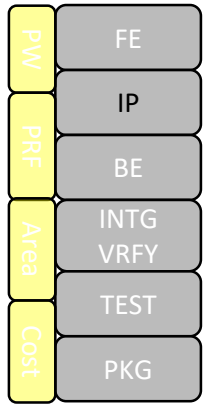
Fundamental IP

Processors

Analog Blocks

Interface IP

Digital Blocks



Rich pool of silicon-proven IPs across different foundries & process nodes

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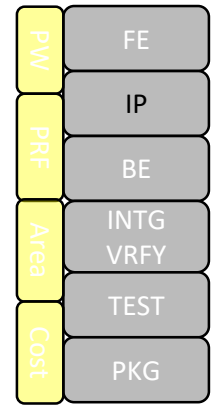
Our IPs Portfolio



Fundamental IP

- Hybrid standard cell library for IoT & battery-powered application
- Memory (foundry-sponsored)
- General Purpose I/O & Special Purpose I/O
- Clock & oscillator (crystal, RC, RTC)
- Power management (DC-DC converter, regulator, LDO)
- PLL (frequency synthesizer, spread spectrum)

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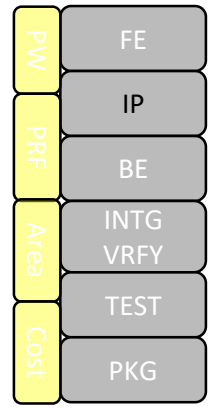
Our IPs Portfolio



Analog Blocks

- SAR ADC (8-bit, 10-bit, 12-bit,14-bit)
- Current-steering DAC (8-bit, 10-bit, 12-bit)
- Audio CODEC (sigma-delta, low power, I2S interface)
- Programmable gain amplifier (PGA)
- LED driver

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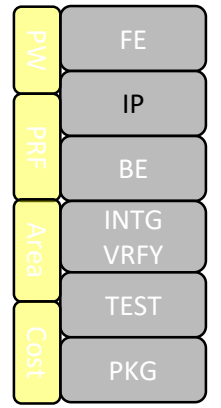
Our IPs Portfolio



Digital Blocks

- UART/USART
- GPIO
- SPI/SSI
- WDT
- I2C
- I2S
- PWM
- Interrupt controller
- RTC
- JTAG
- Bus Matrix
- AMBA 2.0 & 3.0
- DMA controller
- AXI-APB bridge

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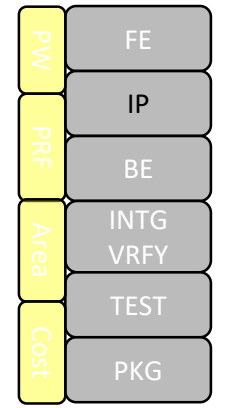
Our IPs Portfolio



Interface IP

- Ethernet PHY
- USB1.1 / 2.0 / 3.0
- PCIe Gen1 / Gen2
- SATA 1.0 / 2.0 (PHY)
- SerDes
- LVDS transceiver
- DDR2, DDR3/3L
- LPDDR2
- SD 2.0 & SD 3.0
- SDIO 2.0 & SDIO 3.0
- Controllers for NAND Flash, CF4.2, AC97 Audio, CMOS sensor interface, TFT/LCD driver interface, LCD image scaling, Infrared wireless serial

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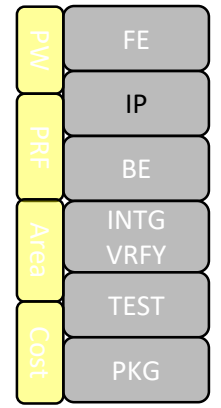
Our IPs Portfolio



Processors

- 8051
- ARM926EJS
- ARM Cortex-M3

We do have a rich pool of silicon-proven IPs across different foundries &
process nodes not limited to the list here.

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Using multi-channel-length approach is optimized for the wearable, mobile and IOT products

Achieve the power goal without changing of the process technology, design flow and redesign of the analog and harden IPs.

MONCLOVA™

low power standard cells library for IoT products