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P&R and Links of FE-BE

March 2019

Moscow

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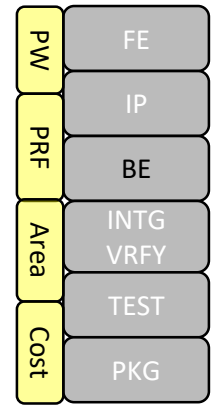
What's in Between



Front-End

A look into some of the works between the 2 major stages

- Physical Design
- Design for Power
- Physical Verification
- SoC Integration & Verification (across FE-BE)

Back-End

Gate-Level Netlist → **GDSII**

Time Lapsed

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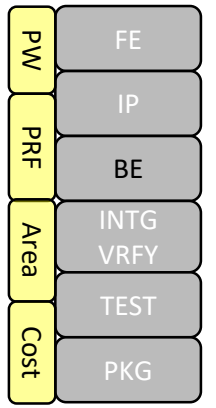
Physical Design



Major physical design topologies for advanced nodes:

- Manufacturing-aware design methodologies
- Process-aware design methodologies
- Interconnect-aware design methodologies

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Physical Design

M-aware

- Multiple-patterning significantly raises the number of extra steps for patterning as well as layout constraints needed for pattern-ability.
- Massive rise in design rules and a loss of achievable (effective) layout density.
- 2D block mask layout for minimum timing degradation, perform placement to fix FEOL & BEOL design rule violation.

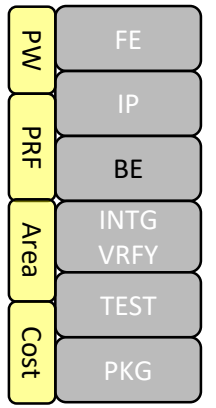
P-aware

- Design variability on process variations has significant impact on the quality and yield.
- optimize top-level clock tree for OCV minimization, reduce skew variation in the clock network and perform partitioning

IC-aware

- Interconnect RC becomes more dominant
- Performance loss from latency increase
- Power increase in net switching
- Area degradation due to rise in buffers & drivers
- Co-optimize wirelength and pathlength in routing

MMMC



Multi-Mode Multi-Corner

What's a Mode

A mode is defined by a set of clocks, supply voltages, timing constraints, and libraries. Covered under SDC file.

What's a Corner

A corner is defined as a set of libraries characterized for process, voltage, and temperature variations that are are not dependent on functional settings; they are meant to capture variations in the manufacturing process and environment in which the chip will operate.

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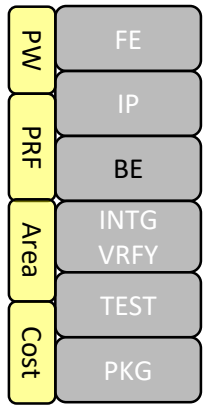

MMMC is increasingly necessary for sub-65nm designs…

1. Close design in different modes:
   - Functional
   - Test (Analog IP) & Loop-back (SerDes)
   - ATPG/SCAN/MBIST
   - Sleep

2. Use STA-like method to concurrently sign-off & optimize design

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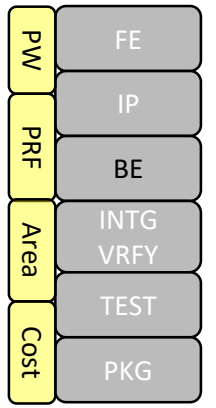

Typical number of cases to close:

- 180nm – 2/3 cases (Best, Worst)
- 130nm – 3 cases (Best, Typical, Worst)
- 90nm – 3/5 cases (+skew corners)
- 65nm & below – 5 & above

And when we don't close all of them…

➔Lots of assumptions made

➔Many missed windows

➔ Sign-off with bigger risk

What if we switch to MMMC?

Reference: http://www.techdesignforums.com

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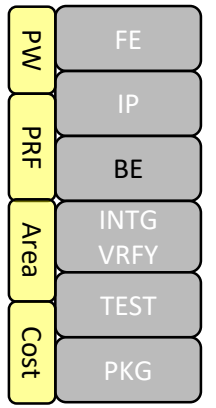
MMMC



Cell Phone Chip

- **Operational Modes**
  - SLEEP (10Khz)
  - STANDBY (10Mhz)
  - ACTIVE (100Mhz)
- **Corner Specification**
  - PVT comers
    - +100C, 1.2V
    - -40C, 0.8V
- **Interconnect corners**
  - MaxR, OCV5%
  - MaxC, OCV12%
  - MaxR, OCV3.3%
  - MaxC, OCV3.3%
  - MaxRC, OCV3.5%
- **Time-to-market — 6 months**

Q: A cellphone chip must have 3 different modes of operation, and satisfy 2 PVT corners and 5 interconnect corners. How many total combined modes/corners we have to run to sign-off?

Ans: Easily 20-30 different mode/corner

"Optimize 1 path violate another scenario.
1 iteration requires 5 RC exrc & 20 STA run."

MMMC reduces run-time by more than 10x

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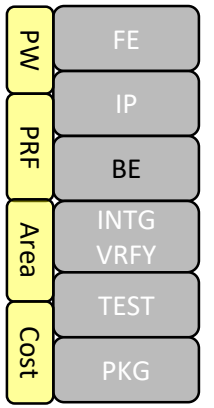
Design for Power



Lower power, smaller battery, lower cost, longer reliability

Typical Design-For-Power flow:

- Application (Conceptual)
- RTL Coding & IP Selection/Design (FE & IP)
- Energy profiling & Optimization (HW/SW Co-DV)
- Power saving mode (FE & Integration)
- ULP flow (Physical design)

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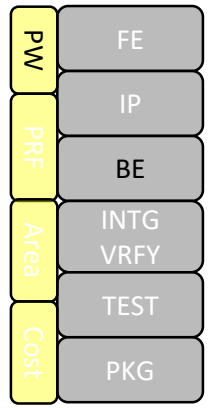
PT (POWER)



Using PT-PX to sign-off power accurately

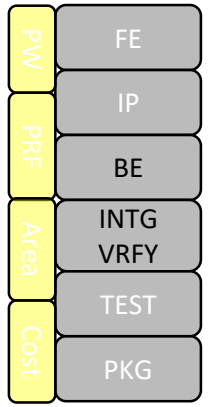
Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	2.614e-03	4.966e-05	2.663e-03	(49.33%)	
memory	0.0000	0.0000	1.647e-04	1.647e-04	(3.05%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	1.503e-03	1.771e-04	4.259e-05	1.723e-03	(31.91%)	i
register	1.192e-05	1.161e-05	6.748e-04	6.983e-04	(12.93%)	
combinational	5.200e-07	3.714e-07	1.489e-04	1.498e-04	(2.77%)	
sequential	0.0000	0.0000	1.560e-07	1.560e-07	(0.00%)	
Net Switching Power	= 2.803e-03	(51.91%)				
Cell Internal Power	= 1.516e-03	(28.07%)				
Cell Leakage Power	= 1.081e-03	(20.02%)				
Total Power	= 5.399e-03	(100.00%)				

Analyze peak & average power, clock network power, and multi-voltage power

- Simulate RTL/GL design on scenarios.
- Ex: reset, sleep, functional
- Generate VCD & SAIF
- Dump & view power waveforms
- Perform power analysis & analyze reports
- Estimate pre-layout clock-tree power
- Annotate clock network power
- Determine savings from clock gating
- Specify PVT corner & libraries

Reference: synopsys

Physical Verification



Difference between DRC, ERC, soft-connect

- DRC/LVS – manufacturing rules, design match
- ERC - checks the violation of electrical rules
- Soft-connect – nets connected via substrate (short)

Common ERC:

- floating NWELL/PWELL
- source & drain connected to power/GND
- floating gate
- floating DNWELL
- NWELL pickup connected to ground
- Hot-well

Soft-check:

- Check for well, substrate, power, ground connections not robust as intended
- Very common found short between digital/analog GND, results in noise coupling

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Thank You