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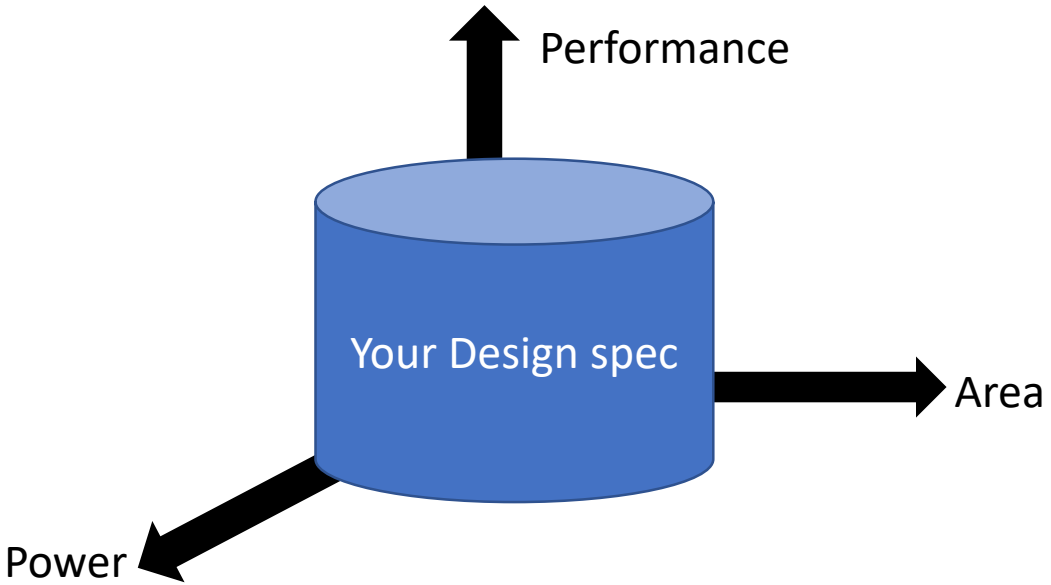
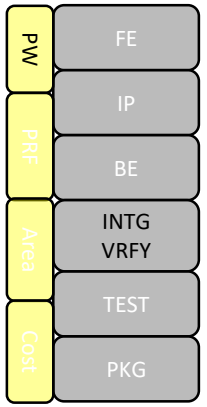
Your One Stop IoT Solution

ASIC/ SoC Integration and Verification

PPA space





Besides on your spec to balanced PPA space.

EX: You want design the max Power .

In the FE begin, you need consider in mind for Power

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Integrate ASIC/SOC

PW PRF Area Cost

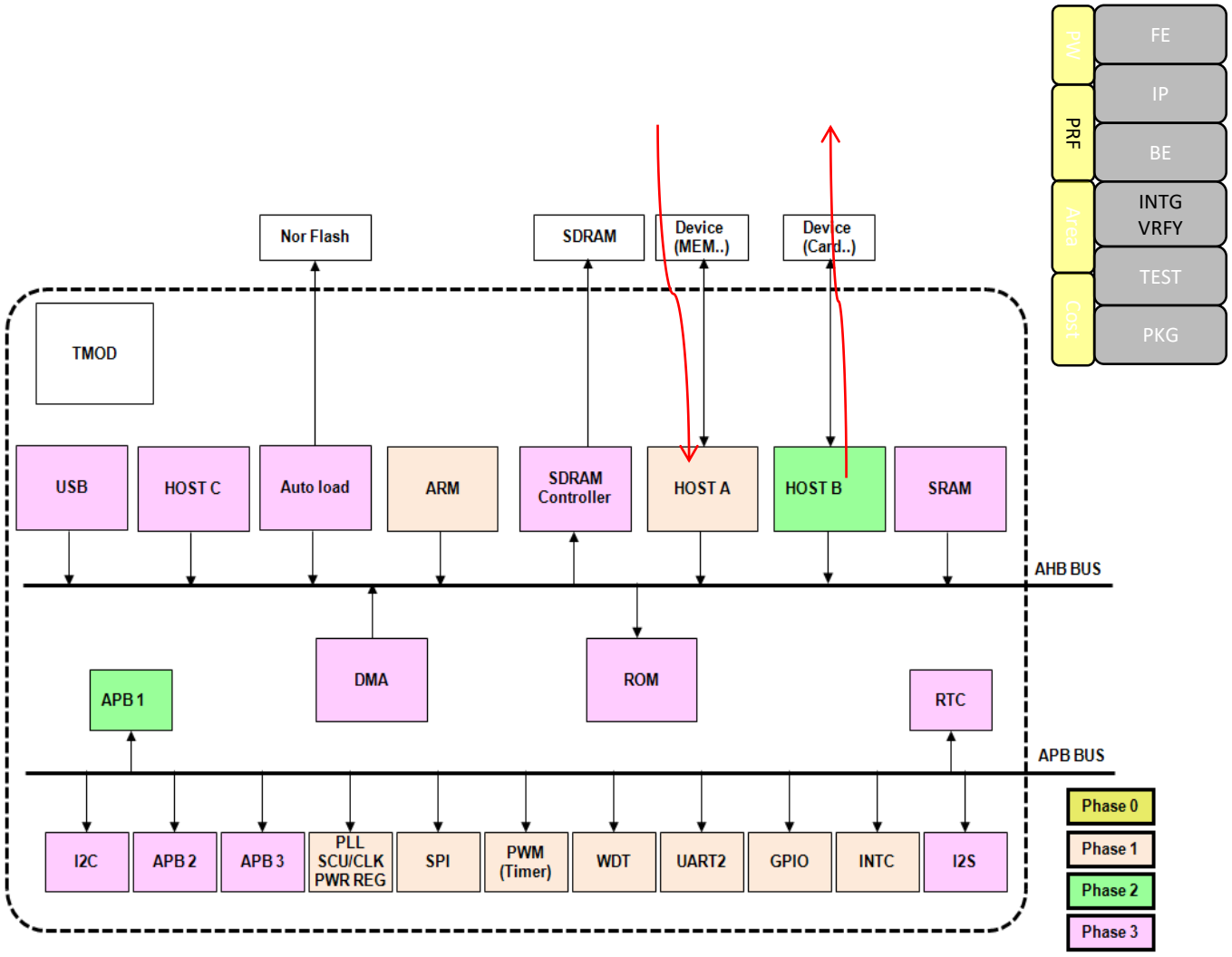
FE
IP
BE
INTG VRFY
TEST
PKG

Always think of how to improve PPA

- Bus performance
- Clock/reset arch plan
- ASIC/SOC boot plan
- Memory usage plan

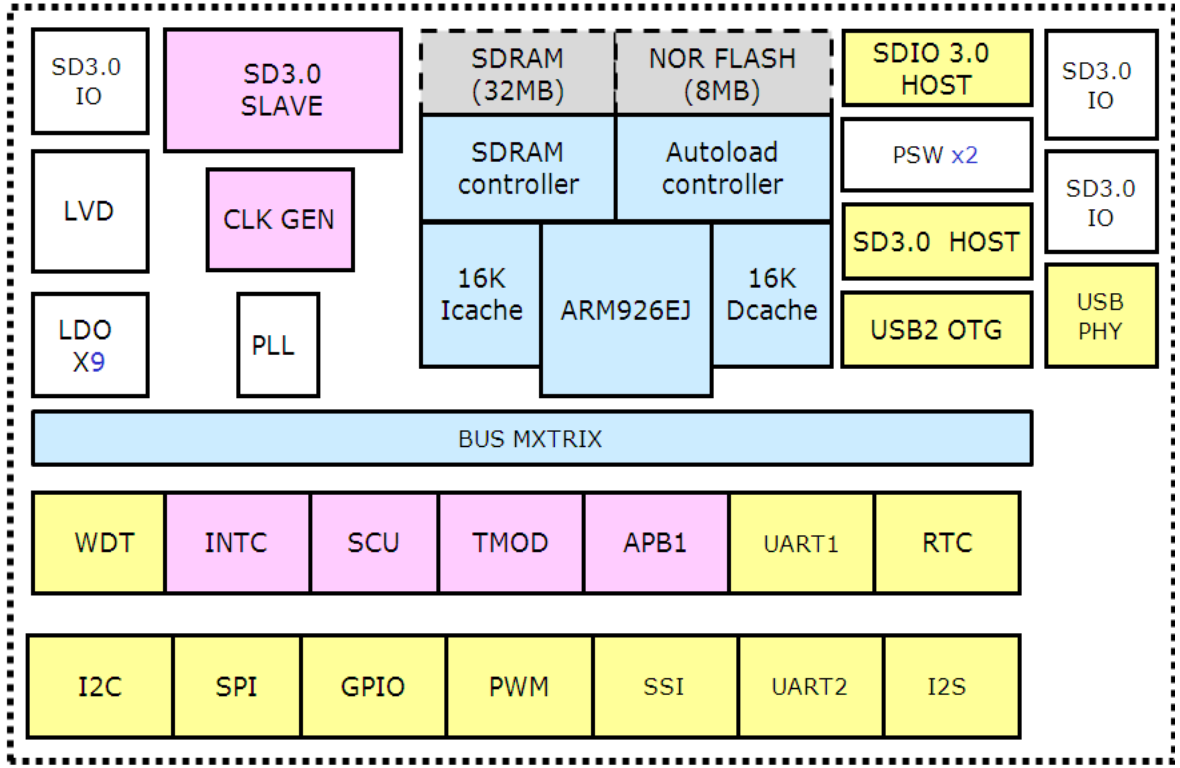
Scenario #1

- Performance issue at Host A.
- Host A want read data form Ext mem from SDRAM Through HOST B to Ext SD Card.
- After analysis with it. We find There have 4 timing path in this critical path. Ext to HOST A . HOST A to SDRAM. SDRAM to HOST B. HOST B to Ext SD.
- After Optimization this arch. We reduce full path from 4 path to 2 path. This could increase 50% performance.



Scenario #2

- After review system power save plan.
- Optimization RTL for Clock Gate.
- Separate to Operate/Sleep/Slow mode for SW Control.
- After Optimization, power is reduce.



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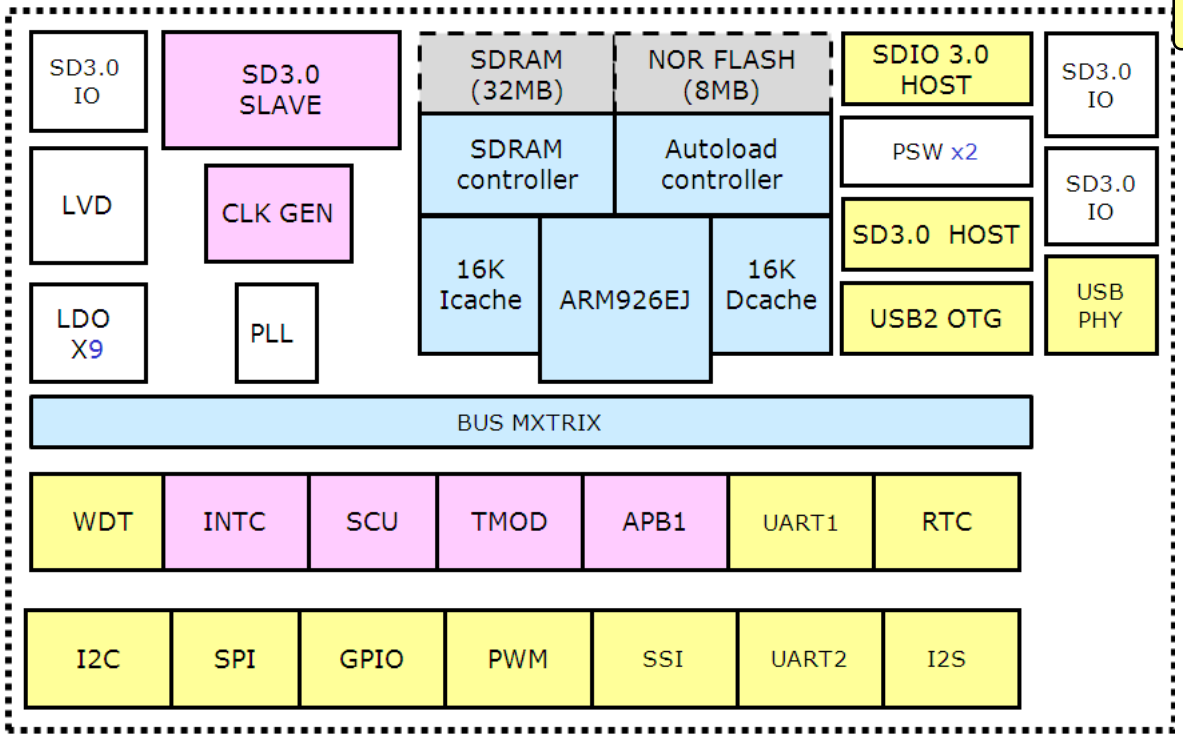
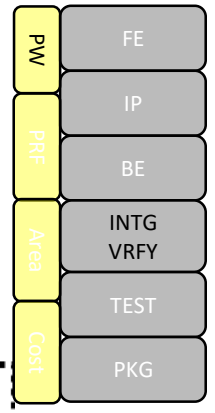
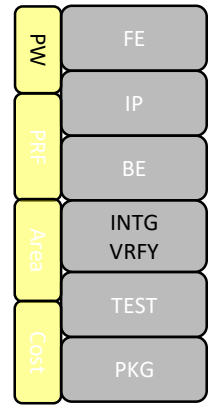
Scenario #3

- There have a power limit in the ASIC Boot up time.
- After review system power usages in ASIC Boot.
- Optimization RTL for System reset control flow.
- Separate reset to HW Boot/SW Boot/Operate mode.
- After Optimization, power is reduce.

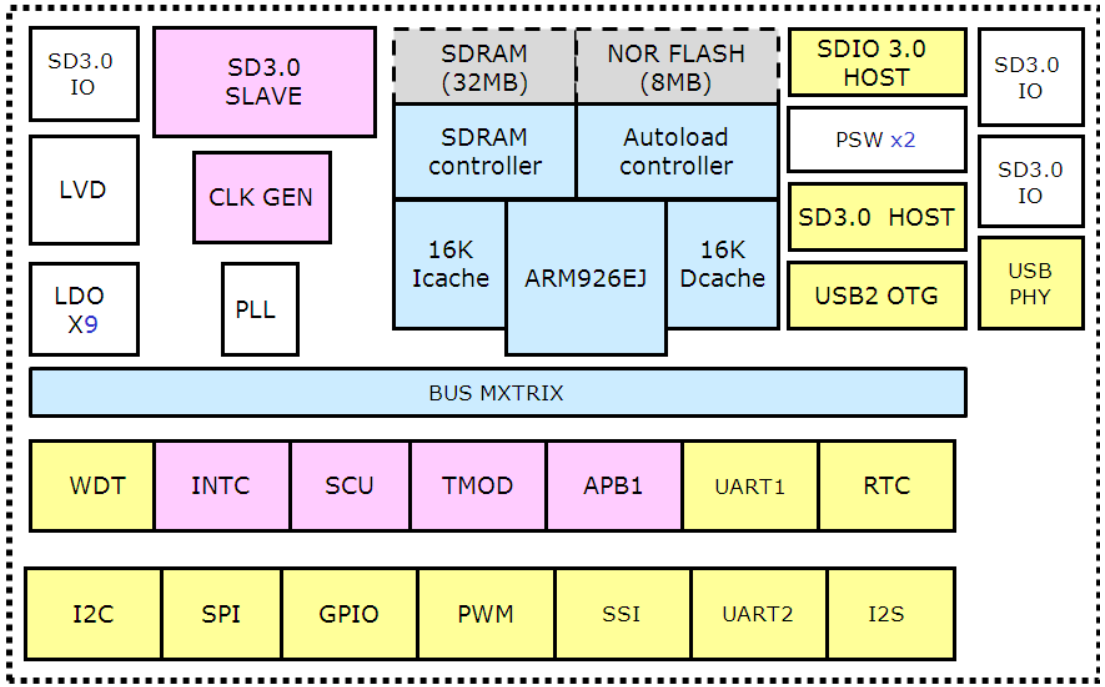




Scenario #2.3



- There are use 16 SRAM on chip.
- After review application use, we optimization RTL for memory number and memory size.
- After Optimization, power is reduce.



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ASIC/SoC Verification

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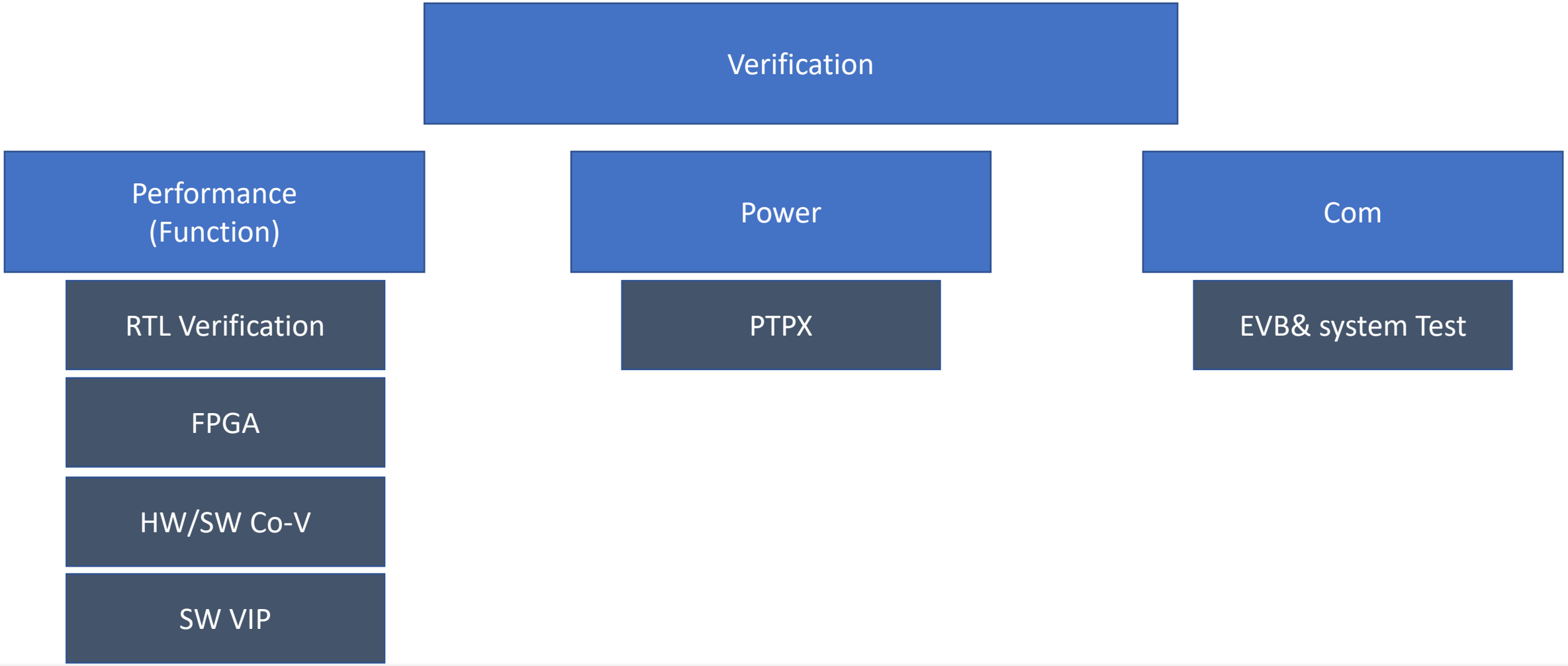
Verification



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Verification

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Always think of how to improve PPA

- HW/SW control flow
- FPGA Verification
- Timing verification
- Chip-level verification

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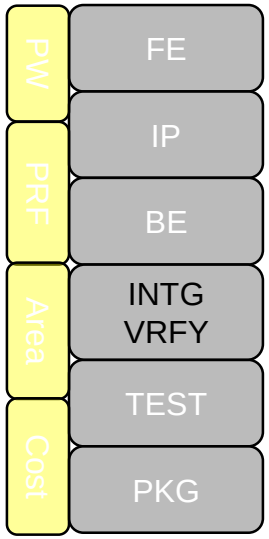
Verification (RTL)



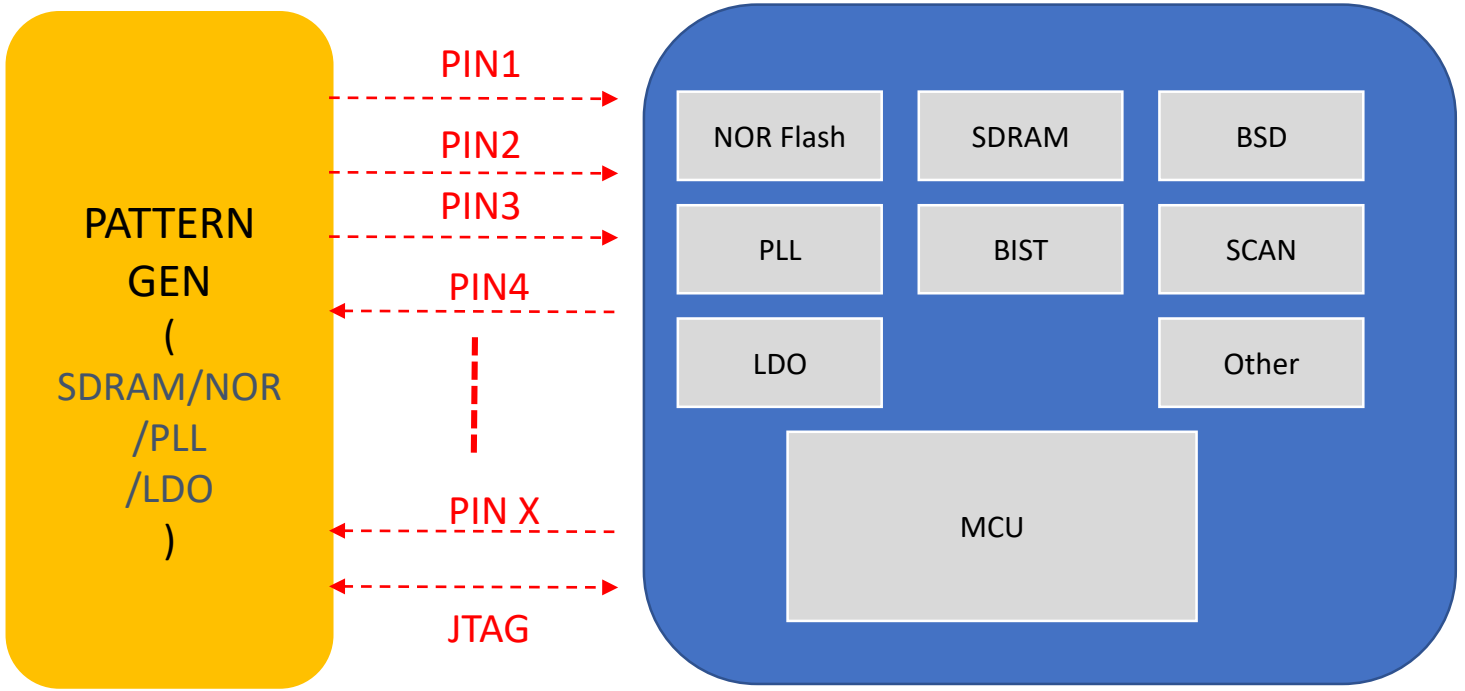
Functional Mode

Test Mode

- Review system Function/TMOD Verification Plan.
- Distinguish Verification for Function/TMOD

Functional & Test Mode

- Review system Function/TMOD Verification Plan.
- There will Separate.
- Verification IP for TMOD.
- Increase ASIC verification Level.

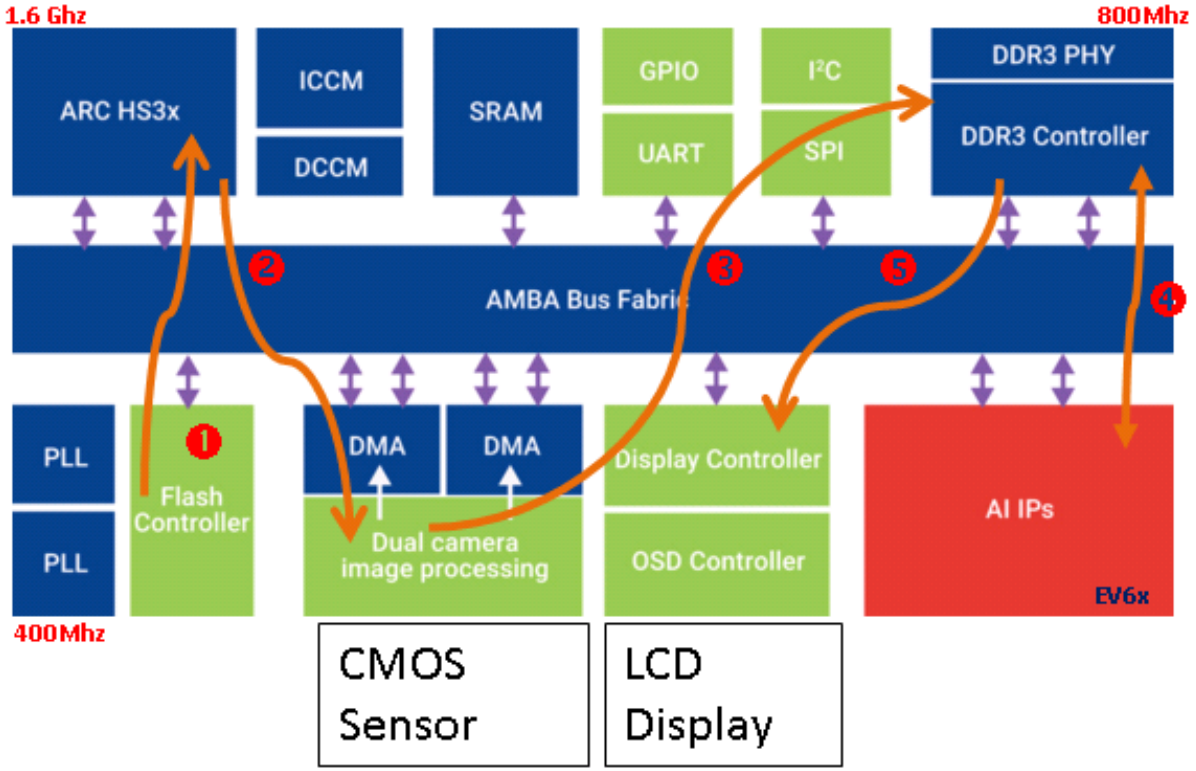


HW/SW Co-V

Where does SW code boot from?

What is the Application?

- Finish HW IP Level Verification.
- Use SW to build up System level Verification.
- Use HW&SW Co-work for Deep System Verification.



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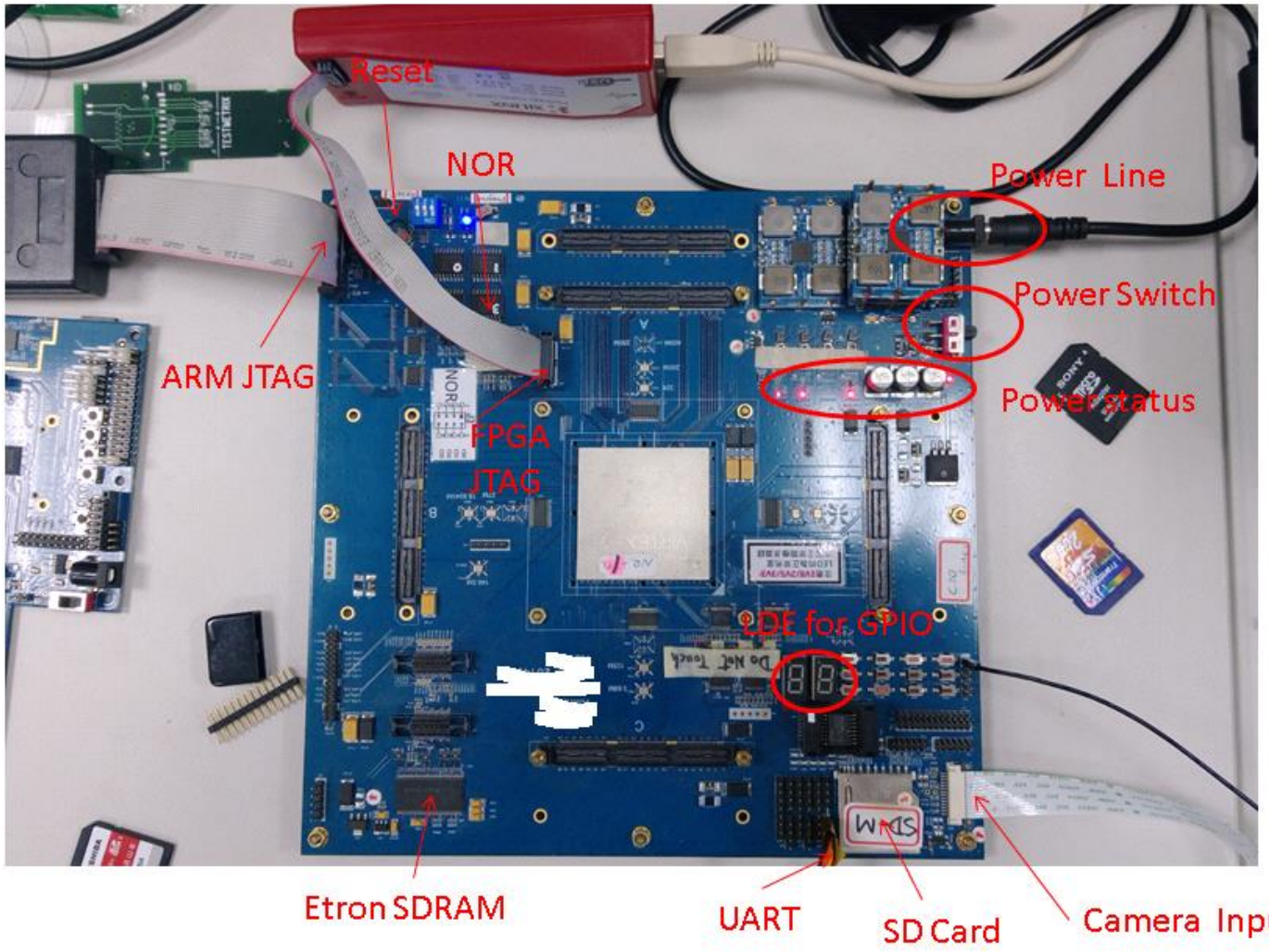
Scenario #4

- This is HW/SW SOC Platform
- ARM C compiler is link with ARM JTAG
- UART could display SW process massage on PC
- FPGA JTAG is use for program SOC Design
- When SOC on, we will program SOC Design and SW



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SW VIP

- KeyASIC FPGA verification program
- Implemented 27+ IPs on SoC FPGA.
- If SOC HW Design have any change. This SW VIP could verification quickly.
- KA also implement Linux base Boot-loader
- New IP verification can be easily integrated in this Boot-loader.

```
======================== KeyASIC Diagnostic Utility Ver 1.1 ==========================

                            ----- System Infomation -----

SoC : P1041C, PCB Ver : 2015/2, Diagnostic Utility Ver : 1.1
Clock(MHz): OSC 24, PLL 96, ARM 96, HCLK 96, PCLK 48, SDM 48, SDSW 48, SDIO 48
PLL2 0, I2S 24, SPI 24
Memory    : 32MB, Clock 96MHz, Vendor : Etron, Model Name : EM63A165GD-10
NOR Flash :  8MB, Vendor : MXIC, Model Name : MX25L6406E

                          ----- IP Verification Tests -----

[ 1]Clock              [ 2]Timer              [ 3]PWM                [ 4]Watchdog
[ 5]GPIO               [ 6]UART               [ 7]DW_UART            [ 8]I2C
[ 9]SDRAM              [10]Mem Ctrl           [11]SRAM               [12]TCM
[13]DW_I2S(*)          [14]SPI/SSI            [15]DW_SPI             [16]SDIO
[17]SD Host            [18]SD Switch          [19]Switch to M1       [20]Switch to M2
[21]DW_DMA             [22]USB2 OTG(*)        [23]Interrupt(*)       [24]Autoload(*)
[25]SPI_SD             [26]GPV(*)             [27]Run All

                                ----- Tools -----

md - read memory          h <1:27> - show help             mmc - mmc subsystem
mm - modify memory        result   - show results          sf  - flash subsystem
mw - write memory         clear    - clear results         icache [on|off]
rd - read register        q        - quit test mode        dcache [on|off]
rm - modify register      m        - back to main menu     reglog <on|off|print|clr>
rw - write register       kamenu   - enter test mode       dmesg  <on|off>
======================================================================================

Select Test (1 - 27):#h 1
```

Power Verification

Power Estimation & Design for Power

- Synopsys PrimeTime–PX.
- Create real application test vector estimation.
- Re-view different Operate mode.

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PT-PX

Check power in term of:

- I/O
- Memory
- Black_Box
- Clock
- Register
- Combo logic
- Report Segmented & total power

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                       0.0000 2.614e-03    0.0221    0.0247 (90.03%)
memory                       0.0000    0.0000 1.647e-04 1.647e-04 ( 0.60%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network             1.503e-03 1.771e-04 4.259e-05 1.723e-03 ( 6.28%)  i
register                  1.192e-05 1.161e-05 6.748e-04 6.983e-04 ( 2.54%)
combinational             5.200e-07 3.714e-07 1.489e-04 1.498e-04 ( 0.55%)
sequential                   0.0000    0.0000 1.560e-07 1.560e-07 ( 0.00%)

  Net Switching Power  = 2.803e-03   (10.21%)
  Cell Internal Power  = 1.516e-03   ( 5.52%)
  Cell Leakage Power   =    0.0231   (84.27%)
                         ---------
Total Power            =    0.0275  (100.00%)
```

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Scenario #6

	Original (TYP)			Optimization (TYP)		
	01_mode	02_mode	03_mode	01_mode	02_mode	03_mode
io_pad	2.662E-03	1.320E-02	2.850E-02	2.662E-03	1.260E-02	2.662E-03
memory	1.647E-04	1.754E-03	2.032E-03	1.647E-04	1.742E-04	1.647E-04
block_box	9.777E-11	7.229E-11	0.000E+00	1.289E-10	1.446E-10	0.000E+00
clock_network	1.842E-04	4.261E-03	2.020E-02	1.842E-04	1.629E-03	1.723E-03
register	5.449E-04	5.823E-04	6.642E-04	5.448E-04	5.720E-04	6.983E-04
combinational	1.485E-04	1.508E-04	2.222E-04	1.483E-04	1.516E-04	1.498E-04
seqential	1.547E-07	3.530E-07	7.130E-07	1-547e-07	1.833E-07	1.560E-07
total power	3.704E-03	2.000E-02	5.160E-02	3.704E-03	1.510E-02	5.398E-03

- Analysis 3 system Operate mode for Estimation detail power information.
- After design optimization. 20mW drop to 15mw . 51mW drop to 5mW.

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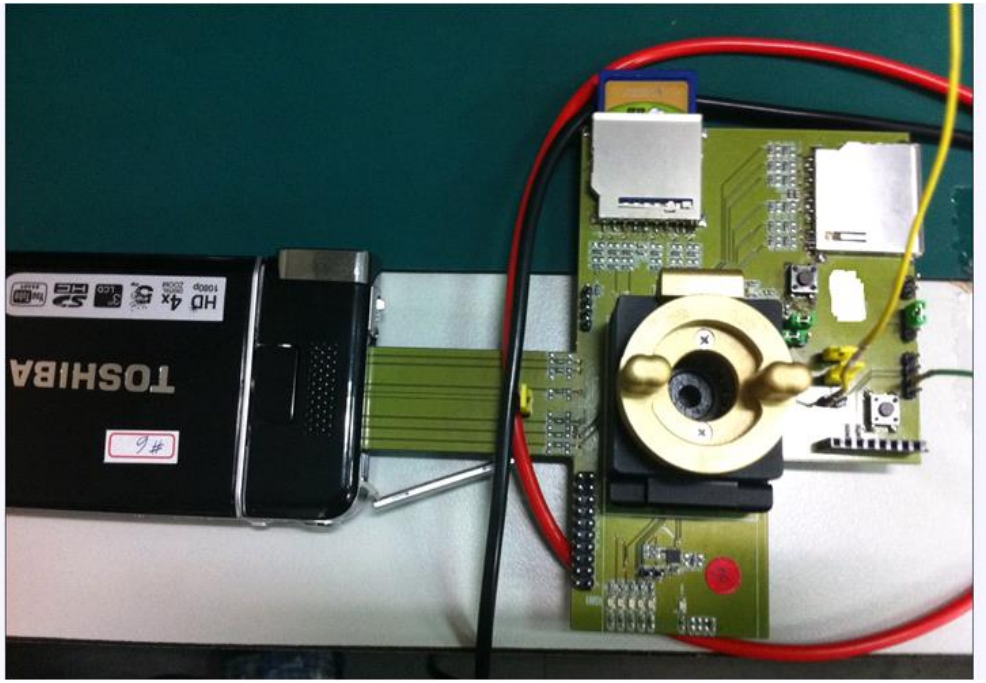
Chip Verification

- Verification with EVB
- Build real application with PCB Environm
- Camera access KA WIFI SOC



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Summary

- PPAC as the key index to measure how good a chip is Besides having the right knowledge & skillset
- Execute your flow with disciplines, always check back against PPAC at any stages!
- A chip design methodology outline is presented and will be covered in details in the coming sessions

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Thank You