Calibre DRC, LVS and DFM overview

Martin Niehoff

Application Engineer Calibre Manufacturing Solutions

January 2019

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Your Presenter – Martin Niehoff

- Graduation from Friedrich-Alexander University (Erlangen-Nürnberg, Germany):
  - Major: Physics - diploma thesis in experimental Optics
  - Minor: Computer Science
- 1998 – 2004: Siemens Semiconductor / Infineon Technologies
  - Metrology process engineering
  - Lithography process engineering
  - Lithography R&D (65nm & 45nm nodes)
- 2004 – 2010: Mentor Graphics
  - European Product Specialist OPC & MDP
- 2010 – 2014: ASML/Brion
  - Senior Application Engineer Fab Tools & OPC
- 2014 – now: Mentor Graphics / Siemens
  - European Application Engineer – Calibre Manufacturing Solutions

Agenda

- Introduction
- DRC, LVS, xRC:
  - Calibre in the EDA Ecosystem
  - Advanced Nodes
  - Established Nodes
  - Productivity
  - Foundry Status
- DFM:
  - LFD
  - YieldAnalyzer
  - YieldEnhancer

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Siemens Investing in Increasing R&D Headcount

Functional Simulation
(Excluding Solido)
+25%

Physical Verification
+15%

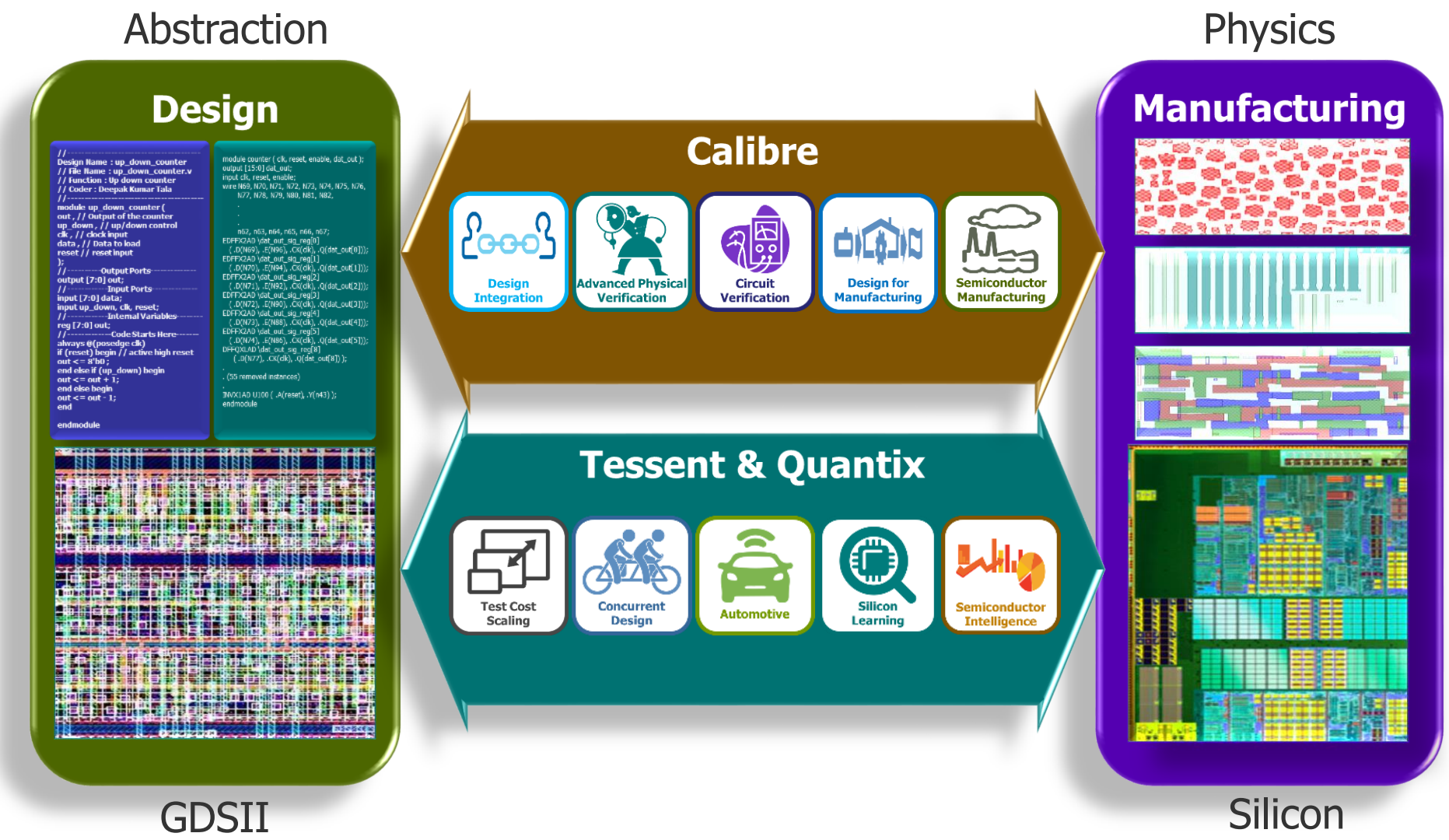
Hardware Based Verification
+33%

Design for Test and Yield
+21%

High Level Synthesis
+33%

All Increases over 20 months
January 31, 2017 through
September 30, 2018

DESIGN TO SILICON



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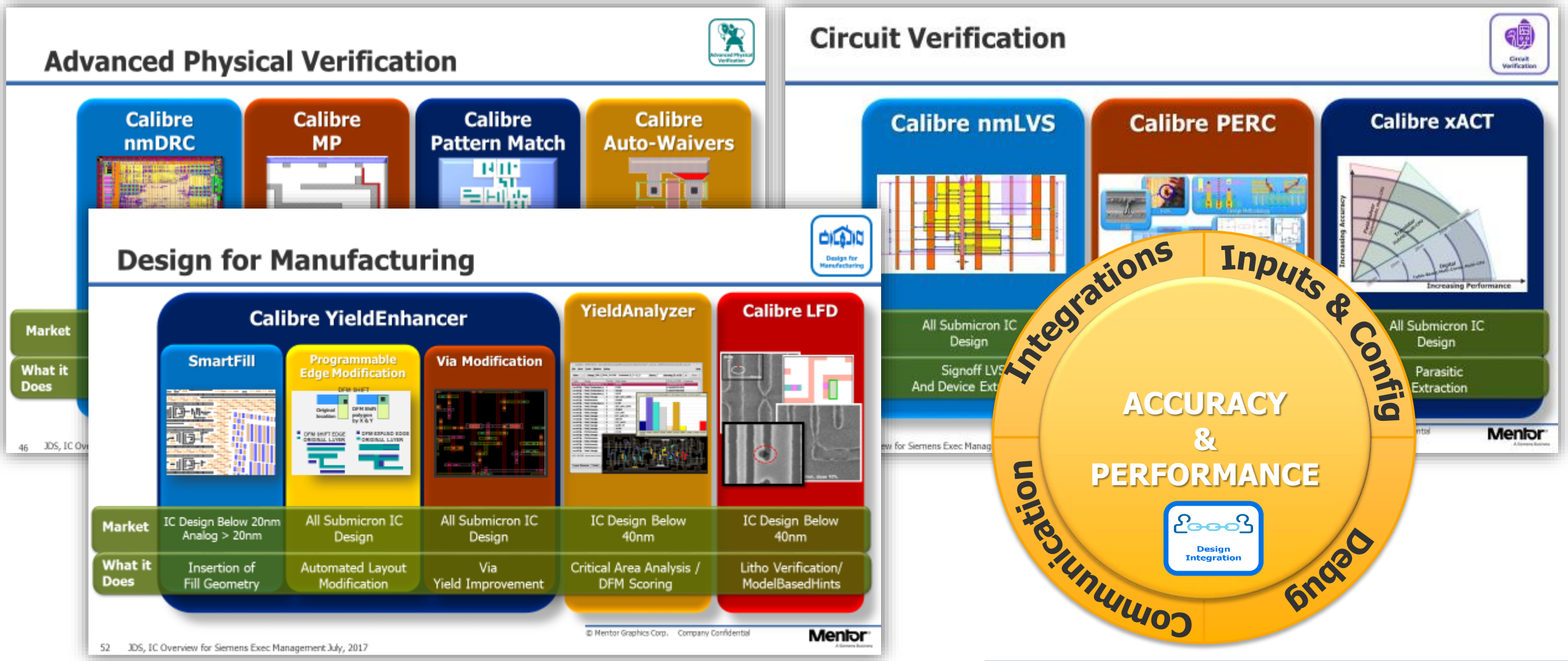
Calibre Design Solutions Portfolio



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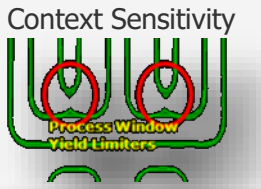
Advanced Physical Verification

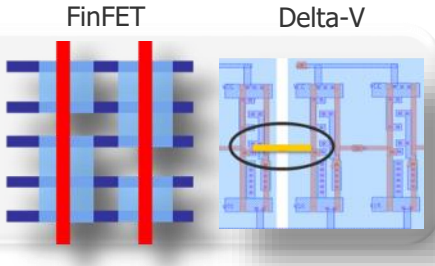
nmDRC/eqDRC

Functionality

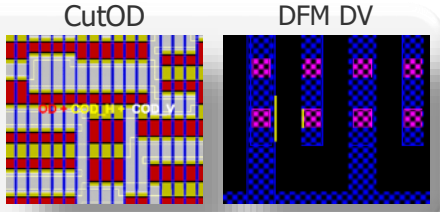
28/22nm



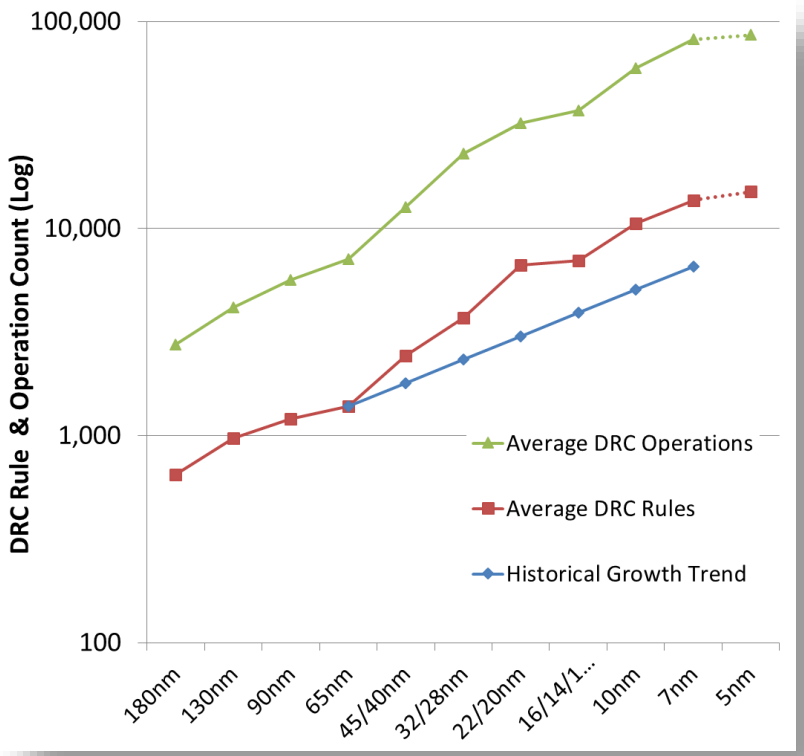
16/14nm



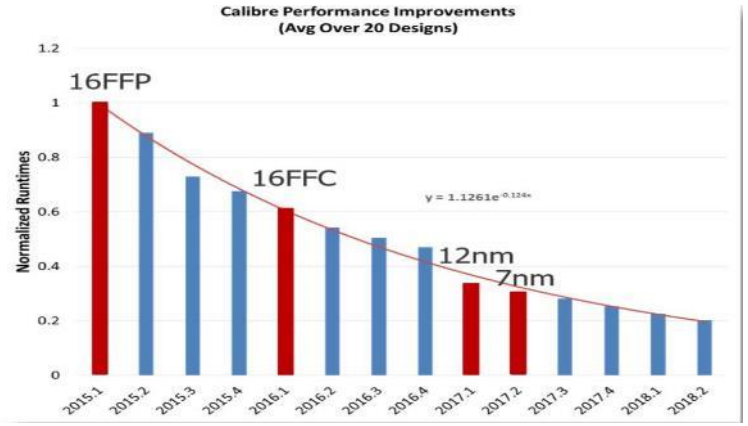
10/7/5nm

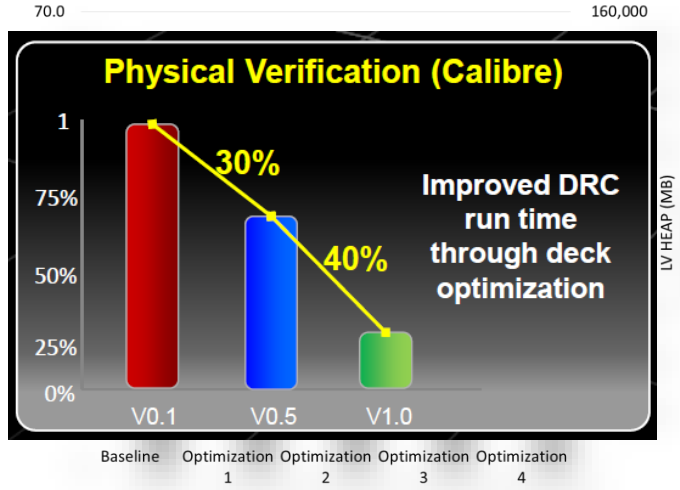


Complexity



Performance





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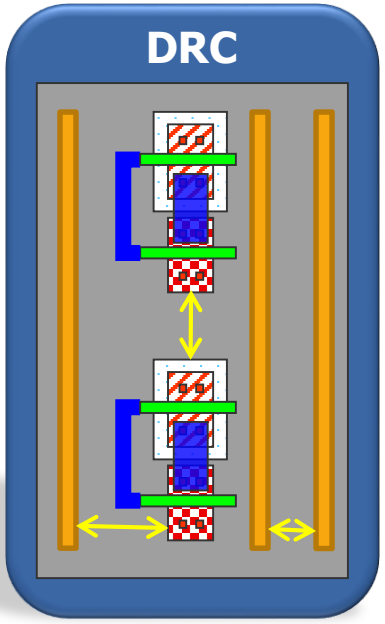
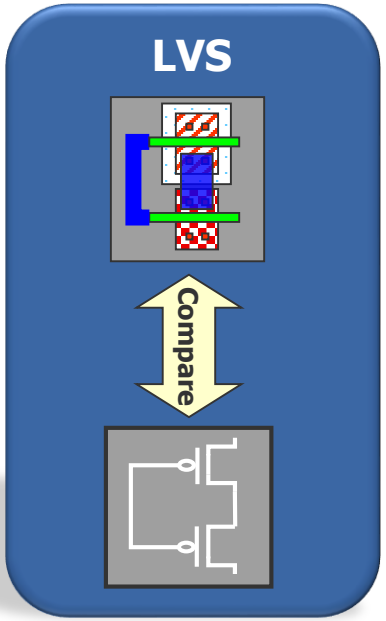
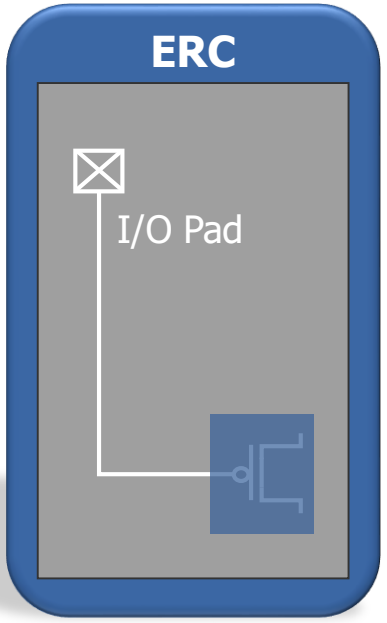
Traditional IC Verification

- DRC, LVS, ERC
  - Provide limited context, rules applied to entire design
  - Often leverage "marker" / CAD layers to refine checking area
- Increased design complexity requires focused verification







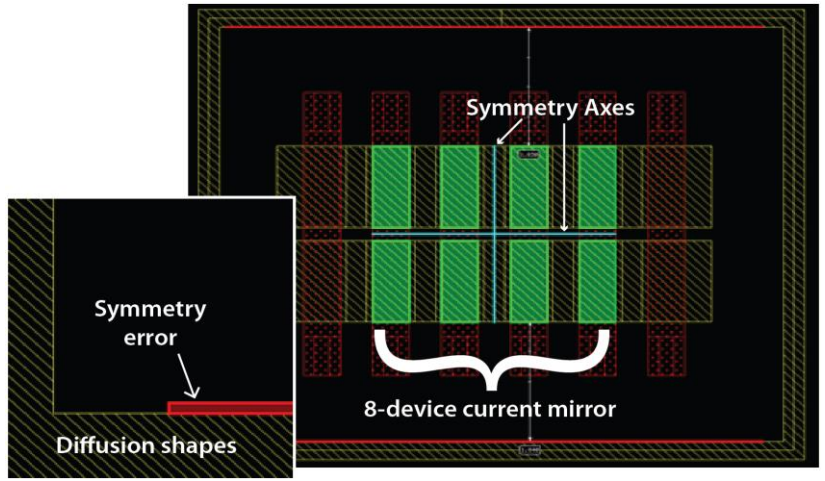
TSMC ESD/Latch-up Rules – From Their DRM

- "Un-checkable" with traditional EDA tools
- Includes reliability focused applications
  - Topology, P2P, CD, layout based latch-up
- Decks available for N28 and below

Analog Constraint Checking - RESCAR

- Focused effort to improve reliability of automotive designs
  - Developed through customer collaboration with Mentor for RESCAR project
- Includes checks for
  - Alignment, Symmetry, Matched Orientation
  - Parameter Match, Cluster, Others
- Simple constraint entry greatly simplifies adoption
- Jointly presented at DAC 2014 and ASP-DAC 2015

RES 2.0 CAR
Robustheit im Bereich Elektromobilität



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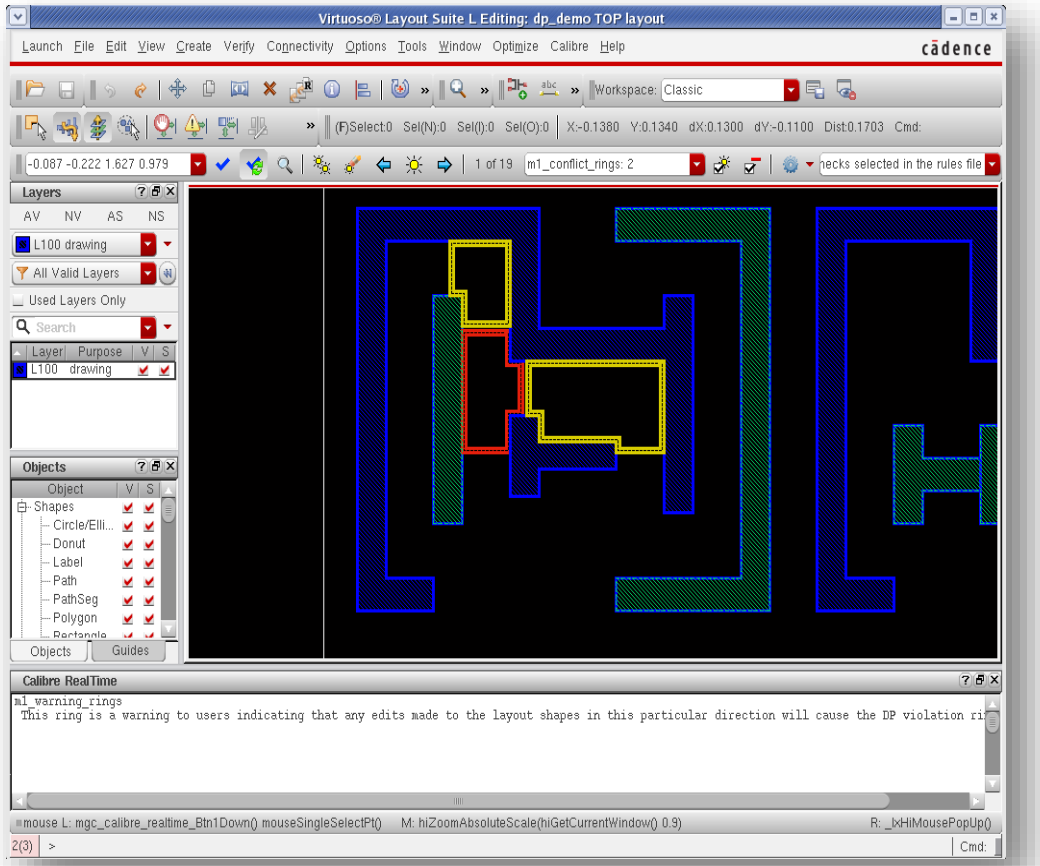
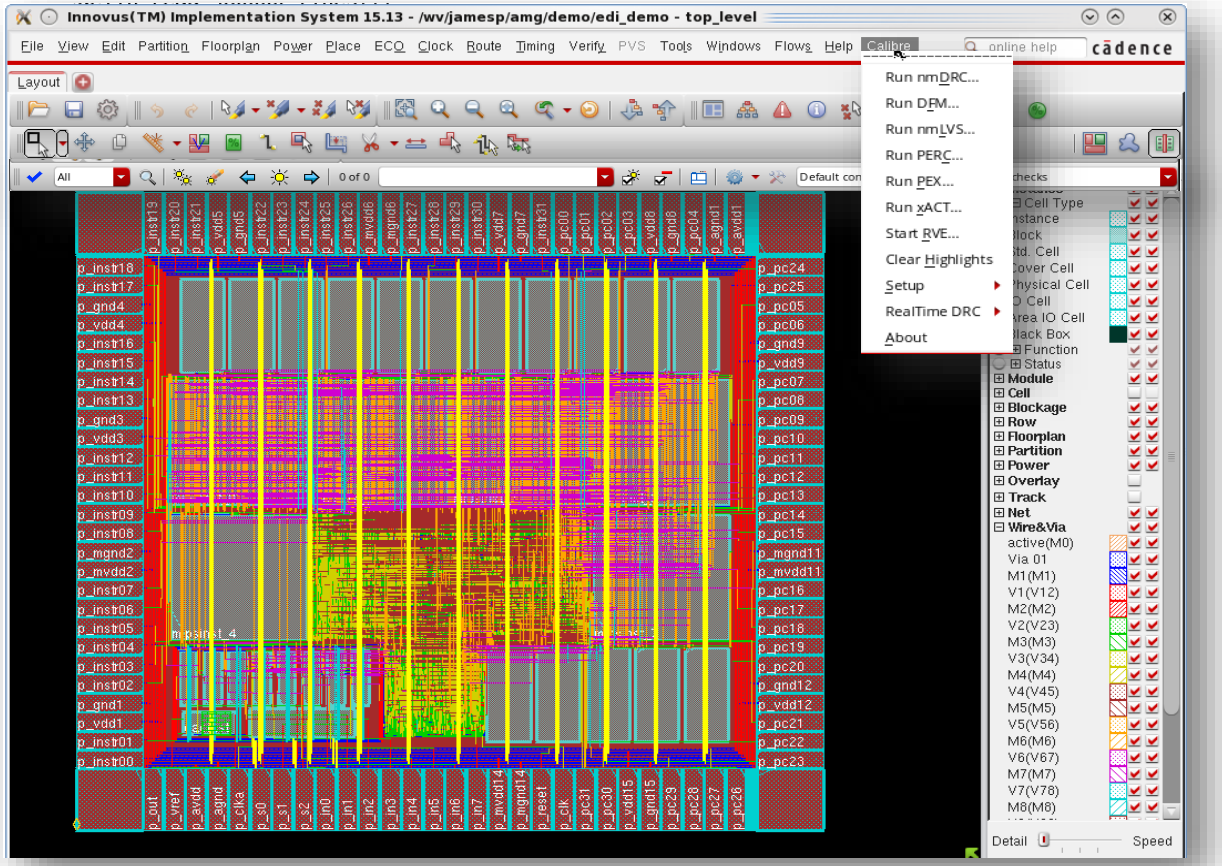
Calibre RealTime Platform: Accelerating DRC Closure



Custom

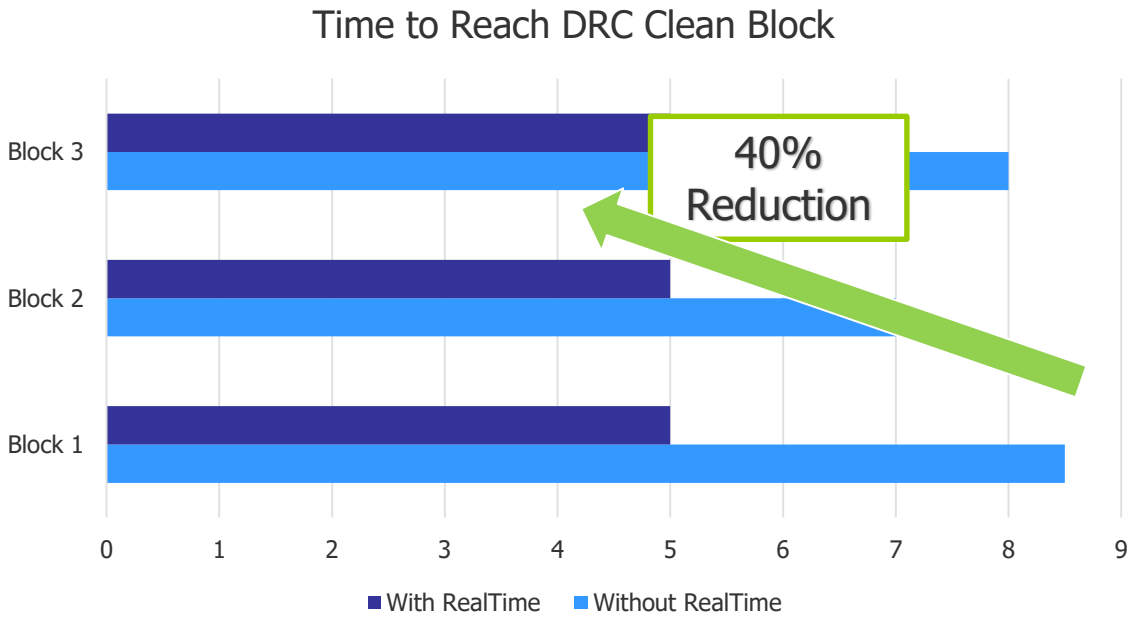
- Interactive checking during design creation

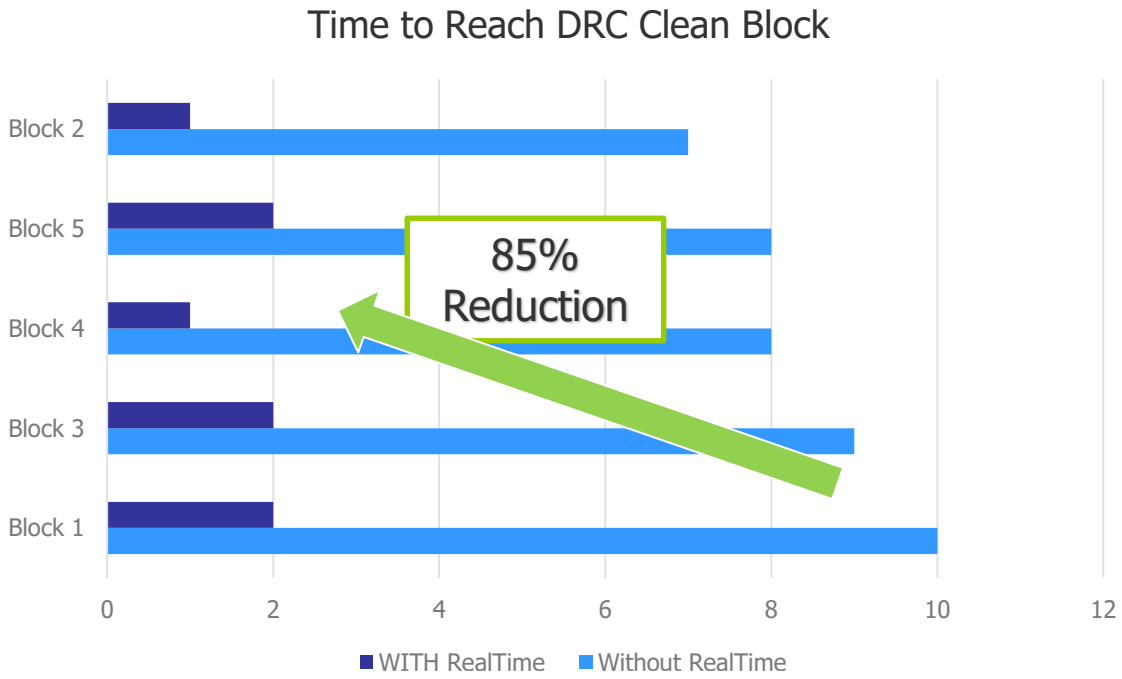


Digital

- Manually fix "Last Few" errors <u>after</u> P&R

Calibre RealTime Digital
Customer Results at Block Level





"40% reduction in DRC closure time for each block @ GF 22nm can save us *2 weeks to Tape-out*

— *Invecas*

"85% reduction in DRC fixing time for every block for every ECO for our 16nm design"

- Customer B

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Calibre Process Support for Established Nodes

Key:	
✓	Golden
✓	Certified
	N/A

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	DRC	LVS	xRC/xACT
130 nm	✓	✓	✓
90 nm	✓	✓	✓
65/55 nm	✓	✓	✓
40 nm	✓	✓	✓
180 BCD/MCU/7HV/WL/7RF/SW	✓	✓	✓
130 BCD/MCU/7HV/WL/7RF/SW	✓	✓	✓
90nm/9SF/9HP	✓	✓	✓
65/55LPe/LPx 10SF/65PKG	✓	✓	✓
45/40nm 45RFSOI/40LP	✓	✓	✓
180 nm	✓	✓	✓
130 nm	✓	✓	✓
110 nm	✓	✓	✓
65 nm	✓	✓	✓
45 nm	✓	✓	✓
HCMOS9gpSOI	✓	✓	✓
65 nm RF	✓	✓	✓

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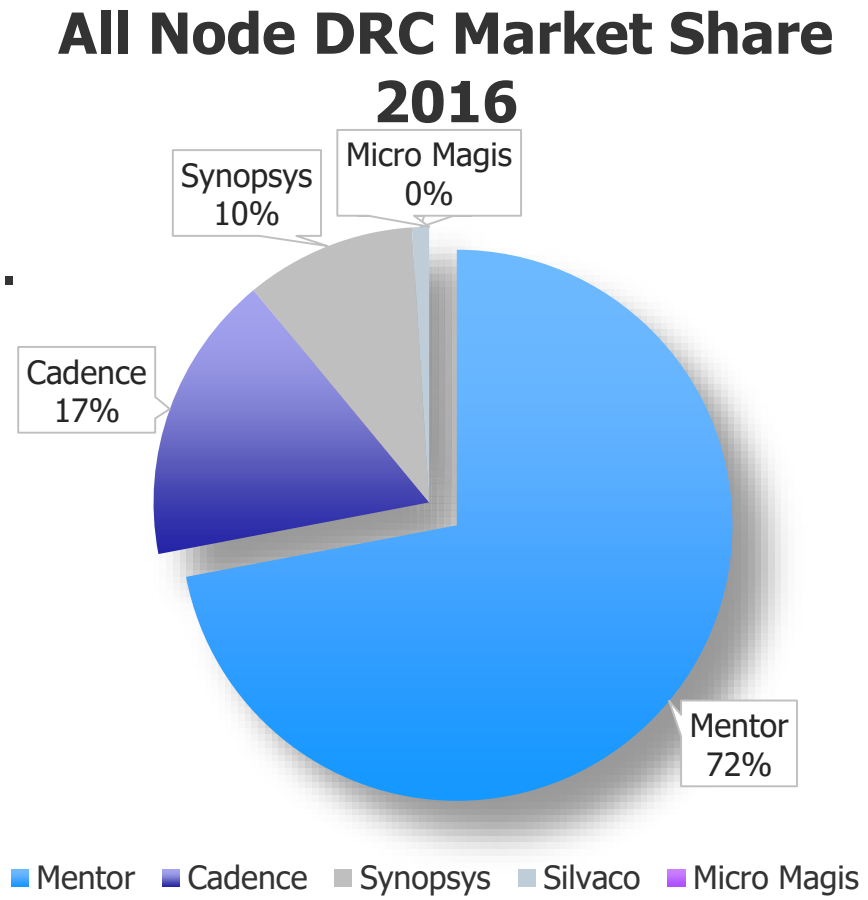
Summary: Calibre is *The* Low Risk Choice

- TSMC Tech Symposium
  - N7: Will tape out ≥50 chips in CY18
  - Using Calibre: 49
- Calibre dominant at: Samsung, GF, UMC, SMIC, etc.
- Integrated everywhere
  - Ecosystem
  - Best in class EDA solutions
- Full solutions, others missing key tools:
  - PERC
  - SRAM/Pattern Matching



Source: Gary Smith EDA (December 2017)

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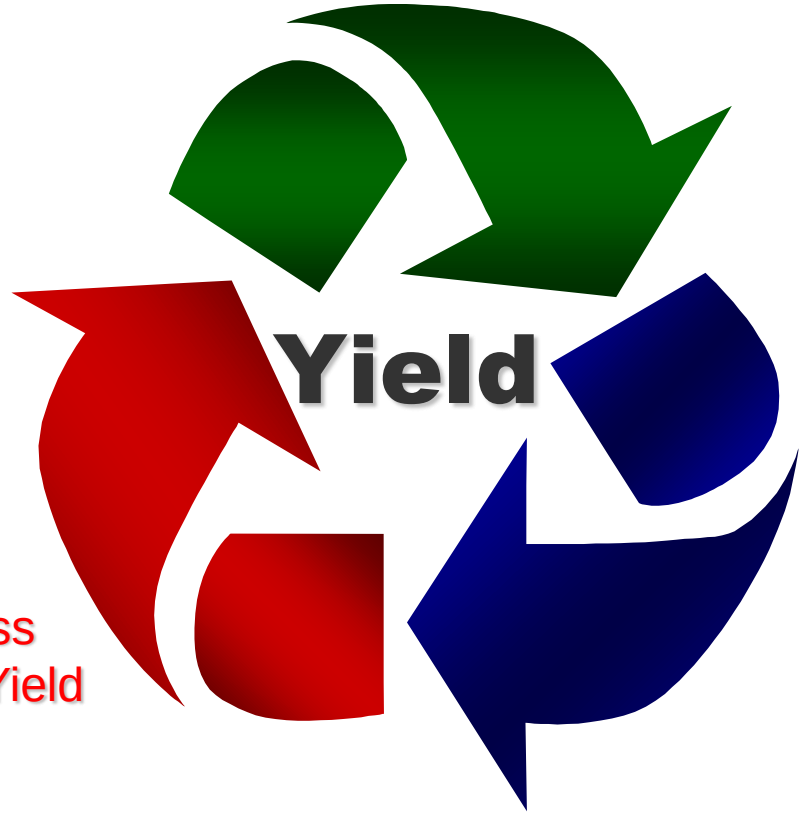
DFM Methodology

Identify

Determine Source, Cause and Impact of Yield Limiters



Enhance

Make Design/Process Changes to Improve Yield

Analyze

Locate, Prioritize and Score the Yield Limiters

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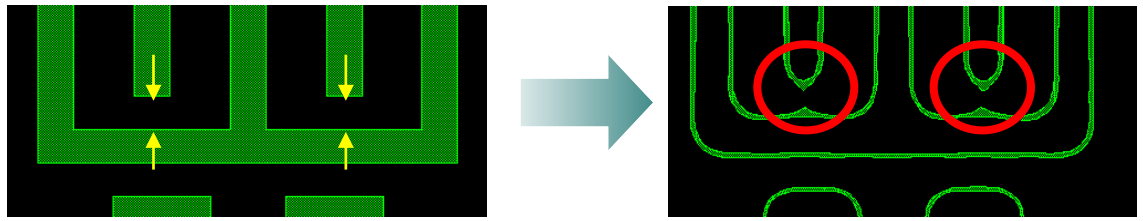
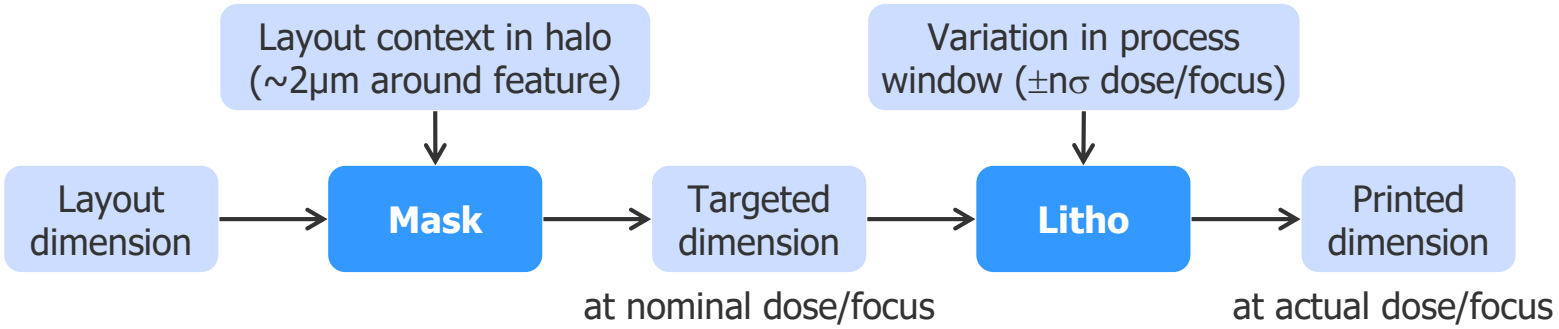
LFD vs DRC

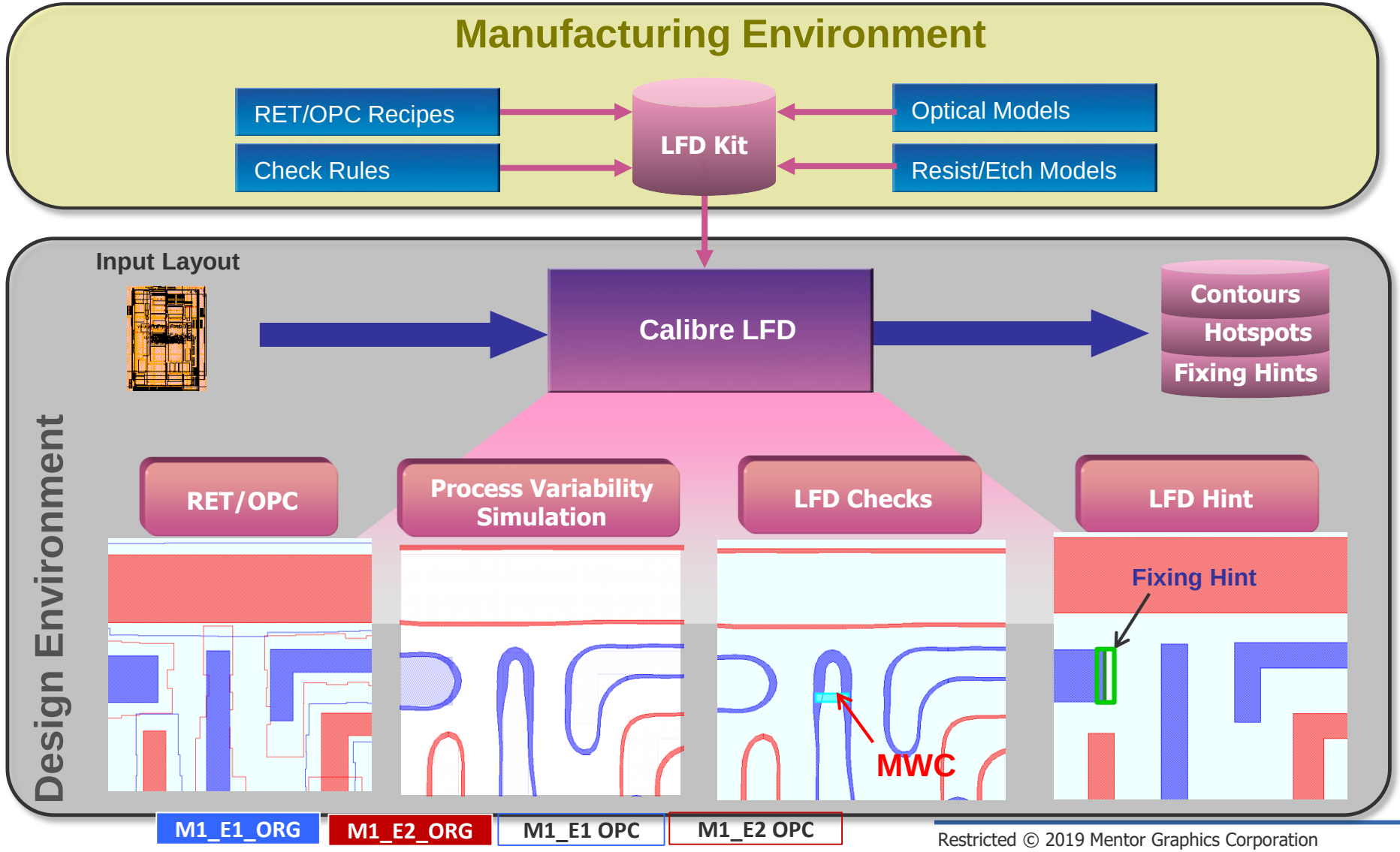
- DRC-clean ≠ printable



Courtesy of Luigi Capodieci, Ph.D. at AMD - SPIE Microlithography 2006



Calibre® LFD: based on production RET/OPC recipes



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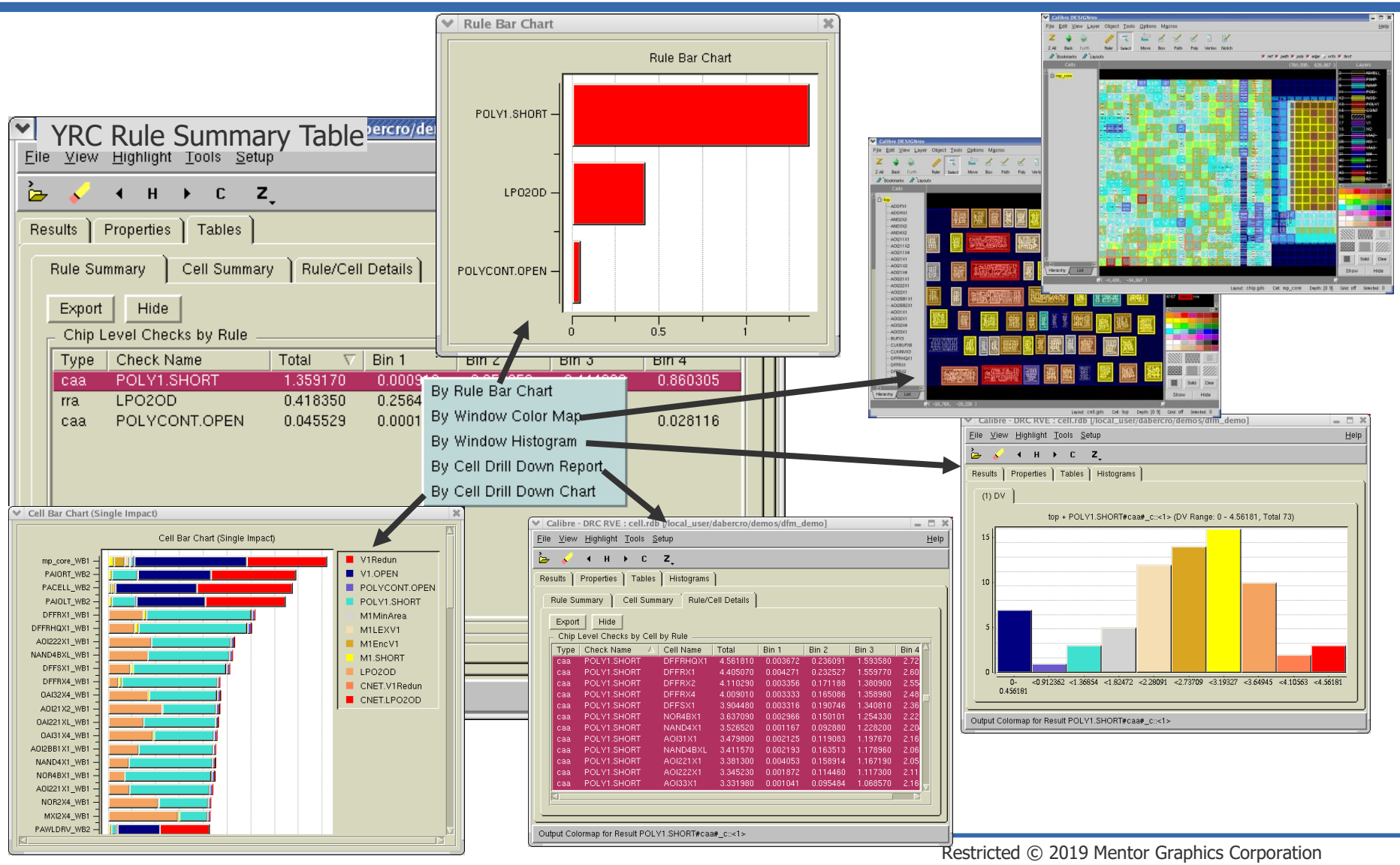
YieldAnalyzer Visualization



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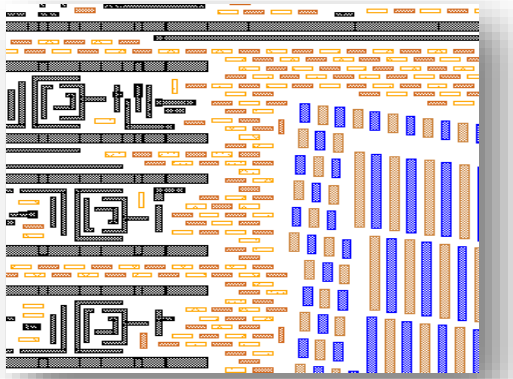
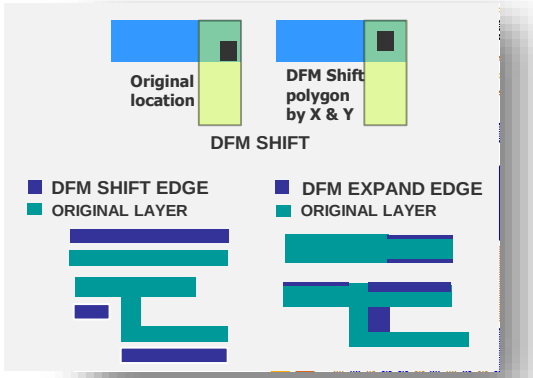
A toolbox for layout modification

- Automatic or user-selected
- DRC-clean and DFM-aware
- Embedded and Programmable features

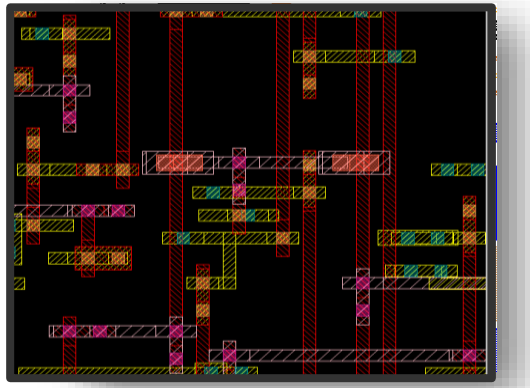
SmartFill



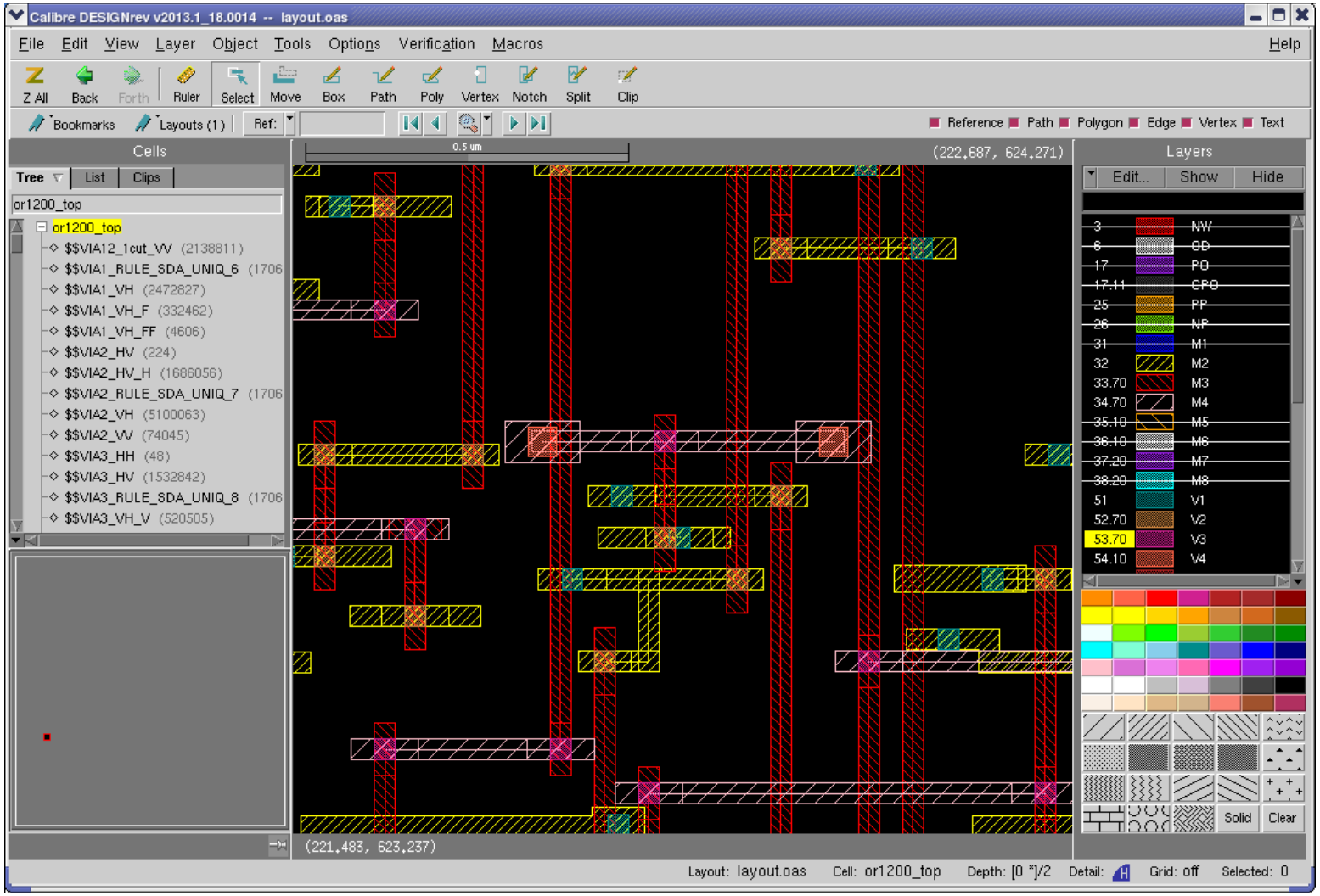
Programmable Edge Movement



Via enhancement



Screenshot before via insertion



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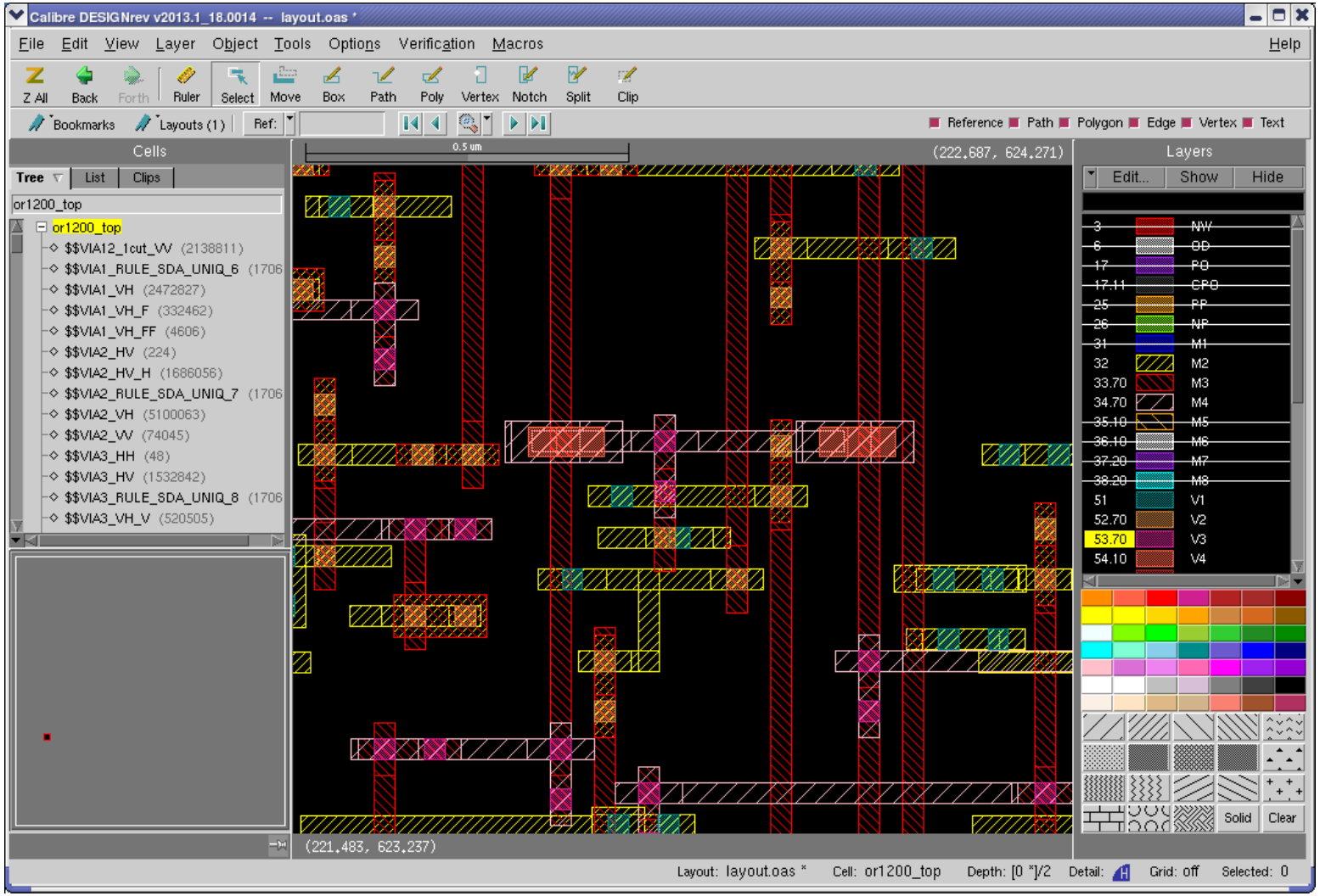
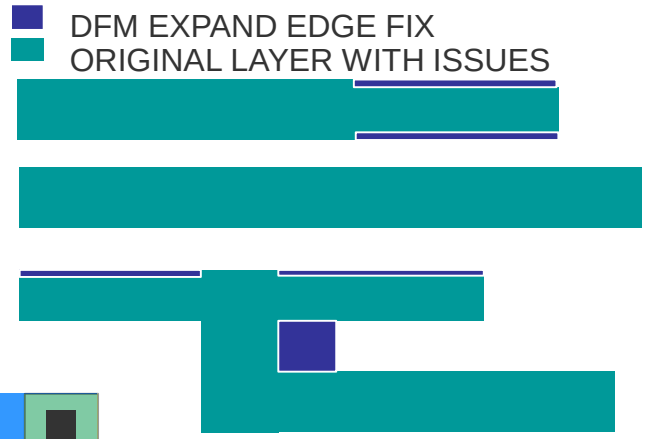
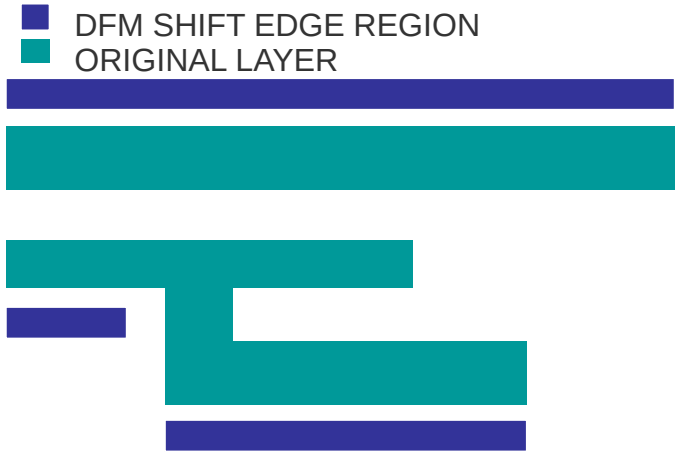
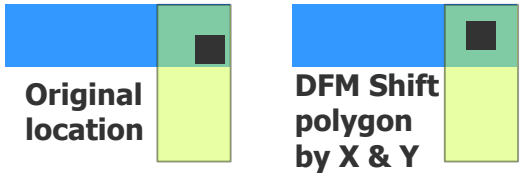


Additional YieldEnhancer Commands: Programmable Edge Movement (PEM)

- Requires deck development
  - Users determine the required movement by analysis
  - Manufacturing companies know from silicon results what changes are needed and by how much to improve Yield
- Released Property Based Edits
  - DFM EXPAND EDGE, DFM GROW
  - DFM SHIFT EDGE, DFM SIZE
  - DFM SHIFT







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