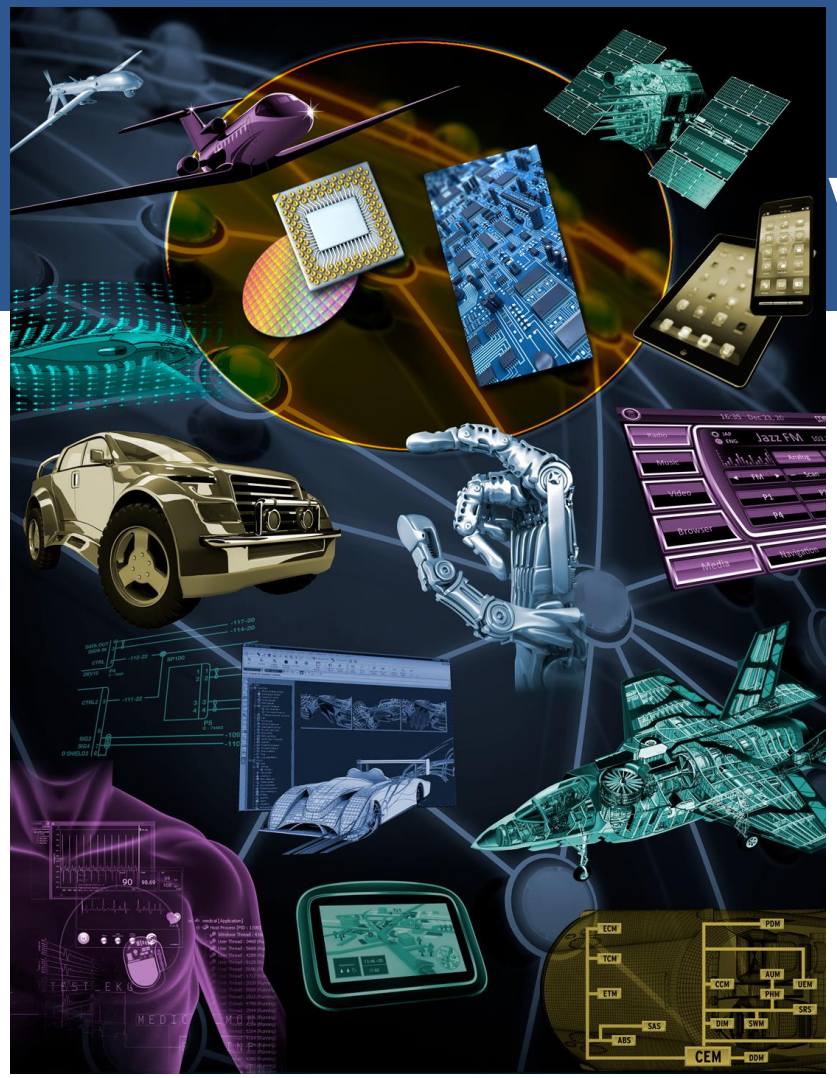


Veloce Technology Overview

Alain Gonier (Application Engineer Manager)
Shaun Bridges (Account Technology Manager)
Romain Petit (Application Engineer)

January, 2019

Veloce STRATO

Mentor®
A Siemens Business

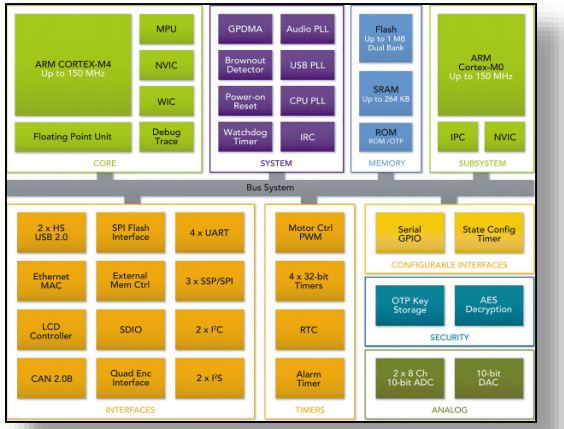
Agenda

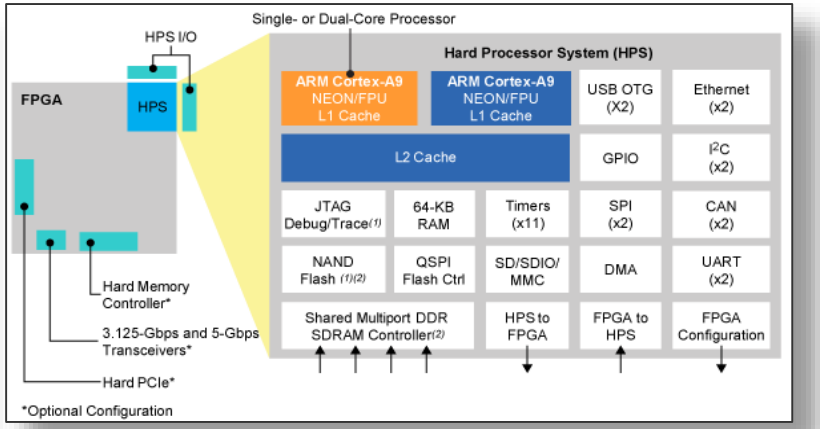
- Intro
- Design & Verification
- Mentor EVP Platform
- Veloce Executive update
  - Siemens Acquisition Update for Mentor Verification and Validation Platform
- Veloce Platform Overview
  - Scalable High Capacity
  - Faster compile
  - Performance measurements
  - Effective Debug
  - Verification Use Modes
  - Applications (Power, Coverage, ES, Automotive, AI/ML)
- Veloce Strato OS overview
- Veloce Apps overview
- Veloce Industry segment solutions overview
- Veloce Customer testimonials

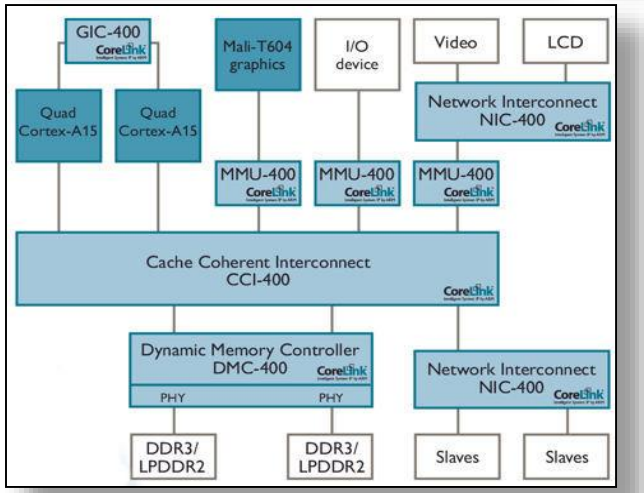
We Live in a System on Chip World

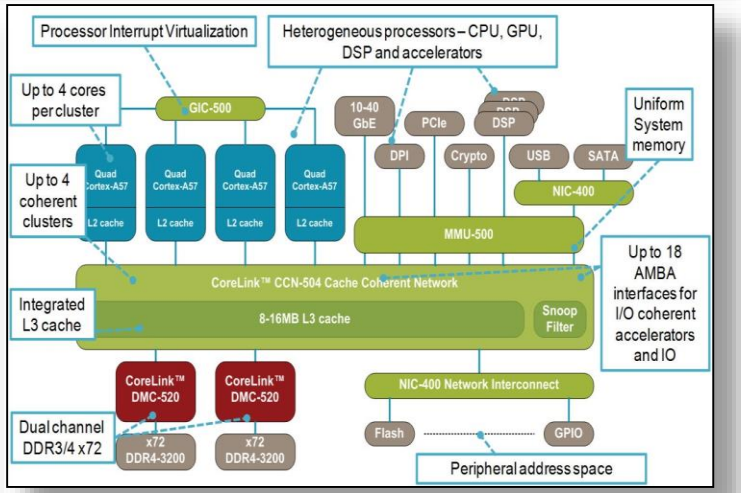
SoC Designs Challenge Verification

- Processors
  - Embedded CPUs, GPUs, & MMUs
- Memory
  - SDRAM, DDRAM, & Cache Layers
- Interconnect
  - Fabrics, Networks, & Bridges
- Peripherals
  - Multiple IP Blocks & Protocols
- Software
  - Instruction Sets & Operating Systems
  - Drivers & Application SW







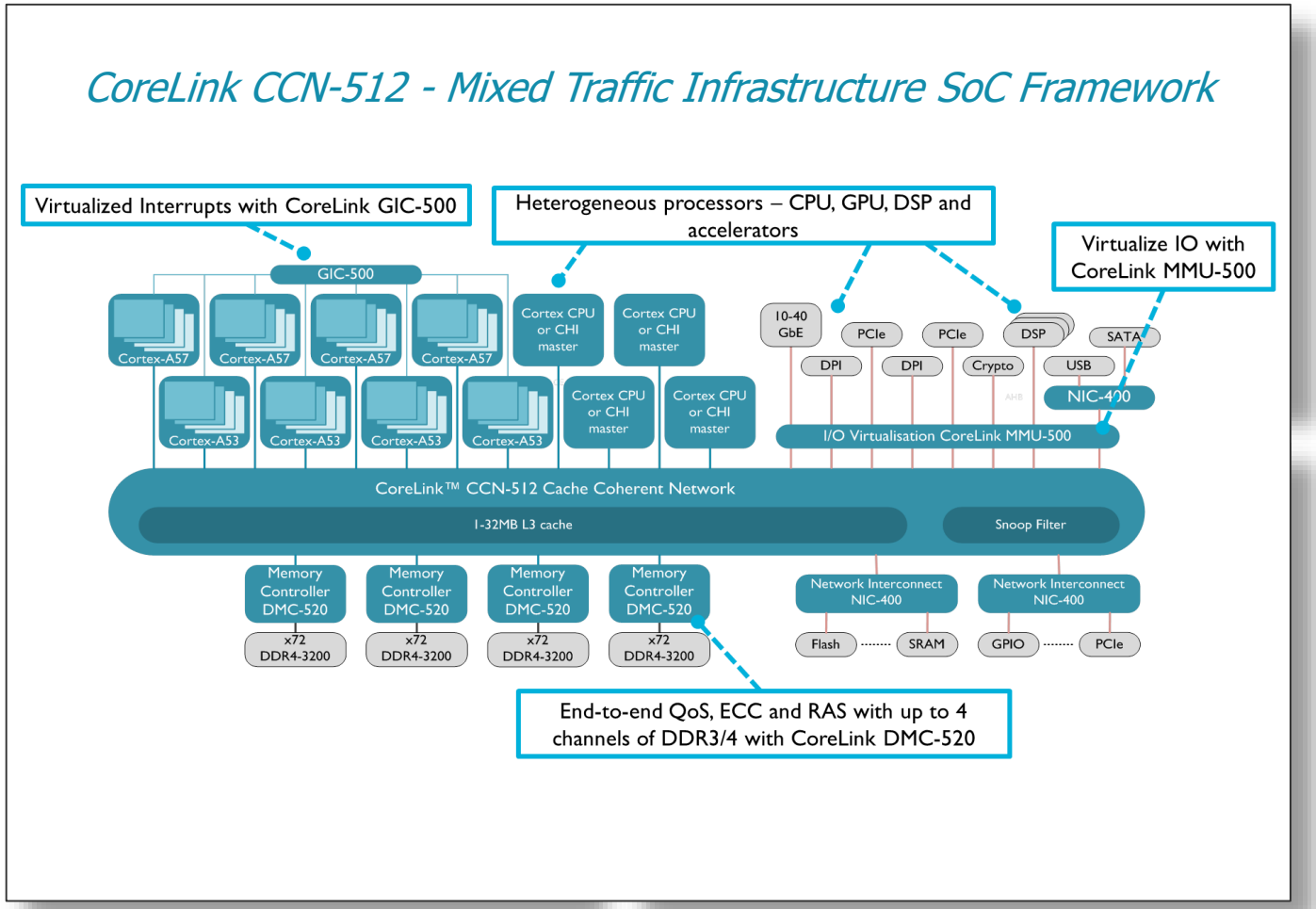


Mentor® A Siemens Business

We Live in a System on Chip World

SoC Designs Challenge Verification

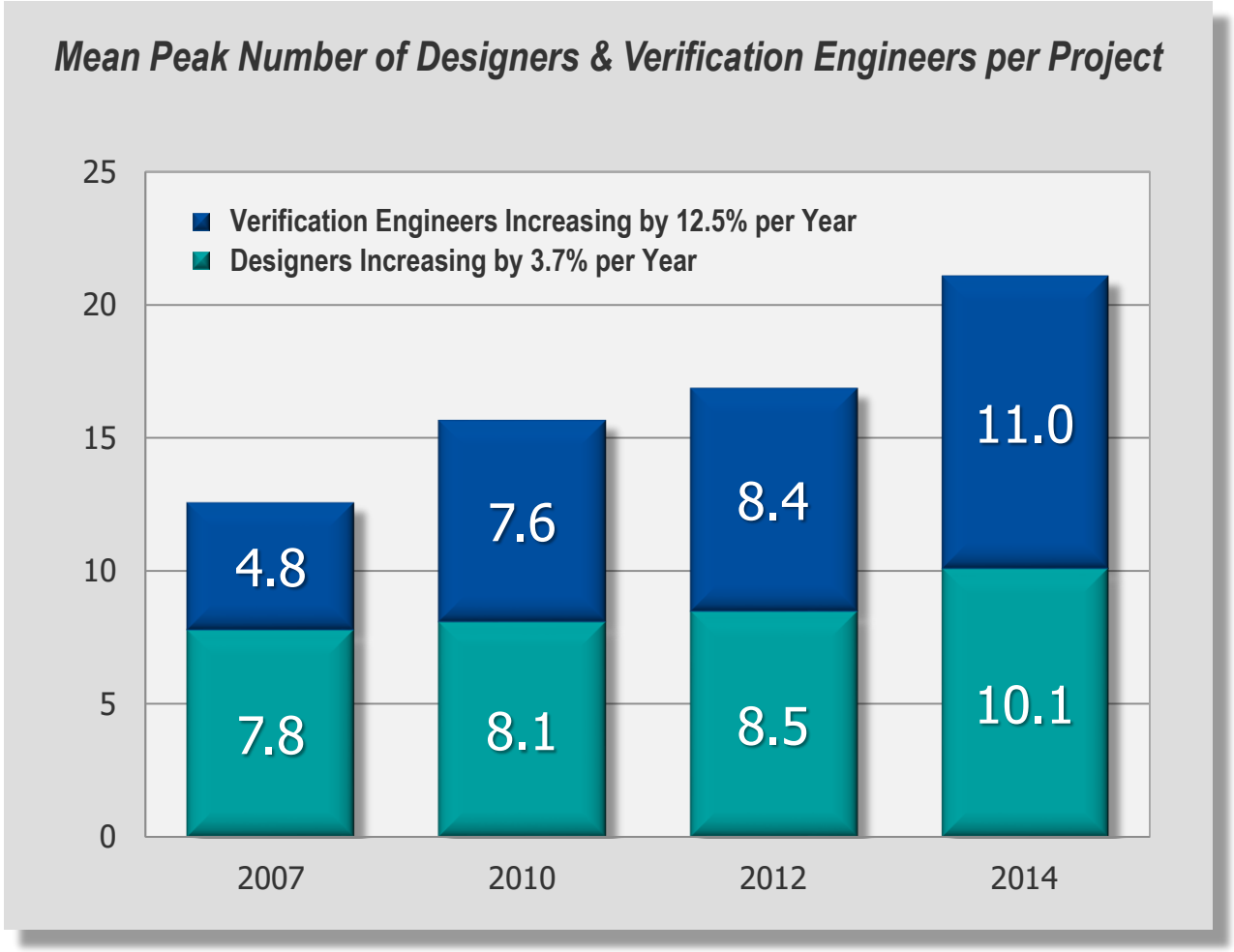
- Processors
  - Embedded CPUs, GPUs, & MMUs
- Memory
  - SDRAM, DDRAM, & Cache Layers
- Interconnect
  - Fabrics, Networks, & Bridges
- Peripherals
  - Multiple IP Blocks & Protocols
- Software
  - Instruction Sets & Operating Systems
  - Drivers & Application SW



Design & Verification

Current Investment Trends Are Not Sustainable

- Verification Engineering
  - Double Digit Growth
  - Investment Eclipses Design

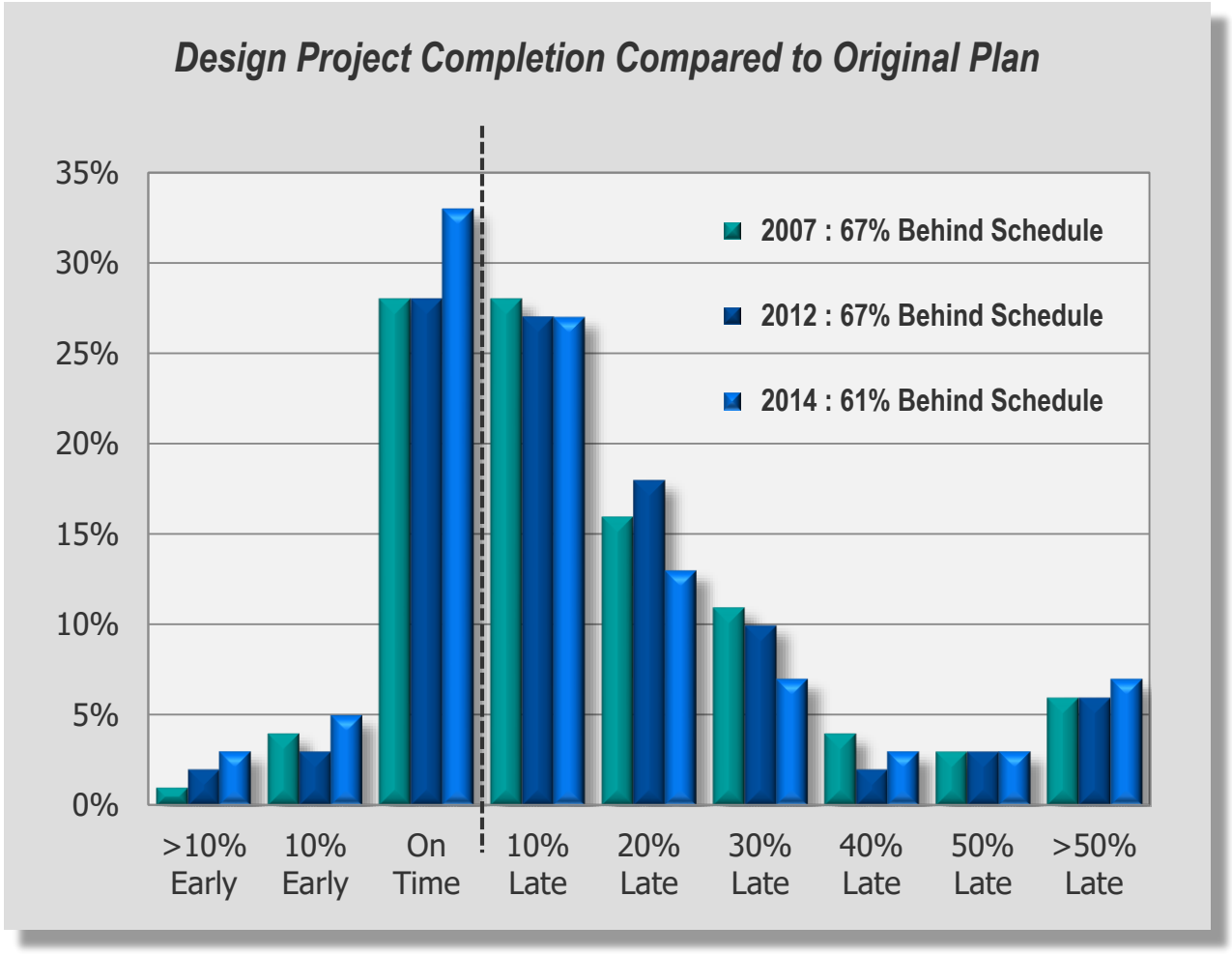


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

Design & Verification

Current Investment Trends Are Not Sustainable

- Verification Engineering
  - Double Digit Growth
  - Investment Eclipses Design
- Design Engineering
  - Spends as much time verifying as designing
- Design & Verification
  - Current Trends Cannot Continue
  - Something Must Change

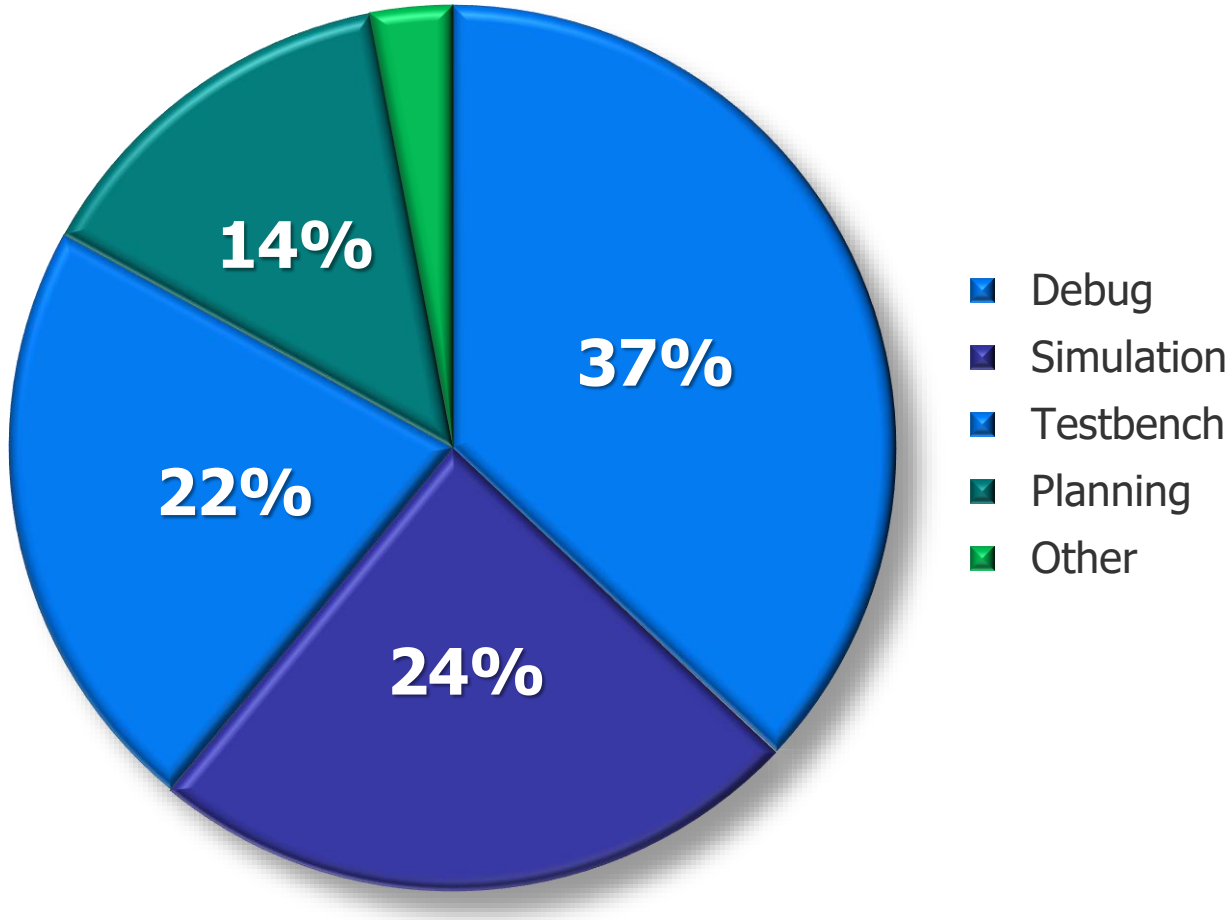


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

Where is Verification Time Spent

SoC Designs Make Existing Verification Challenges More Difficult

- Running Simulation (24%)
  - Speed & Capacity
- Debugging (37%)
  - Power & Predictability
- Testbench Development (22%)
  - Stimulus, Coverage, & Re-use
- Test Planning (14%)
  - Metrics, Analysis, & Process



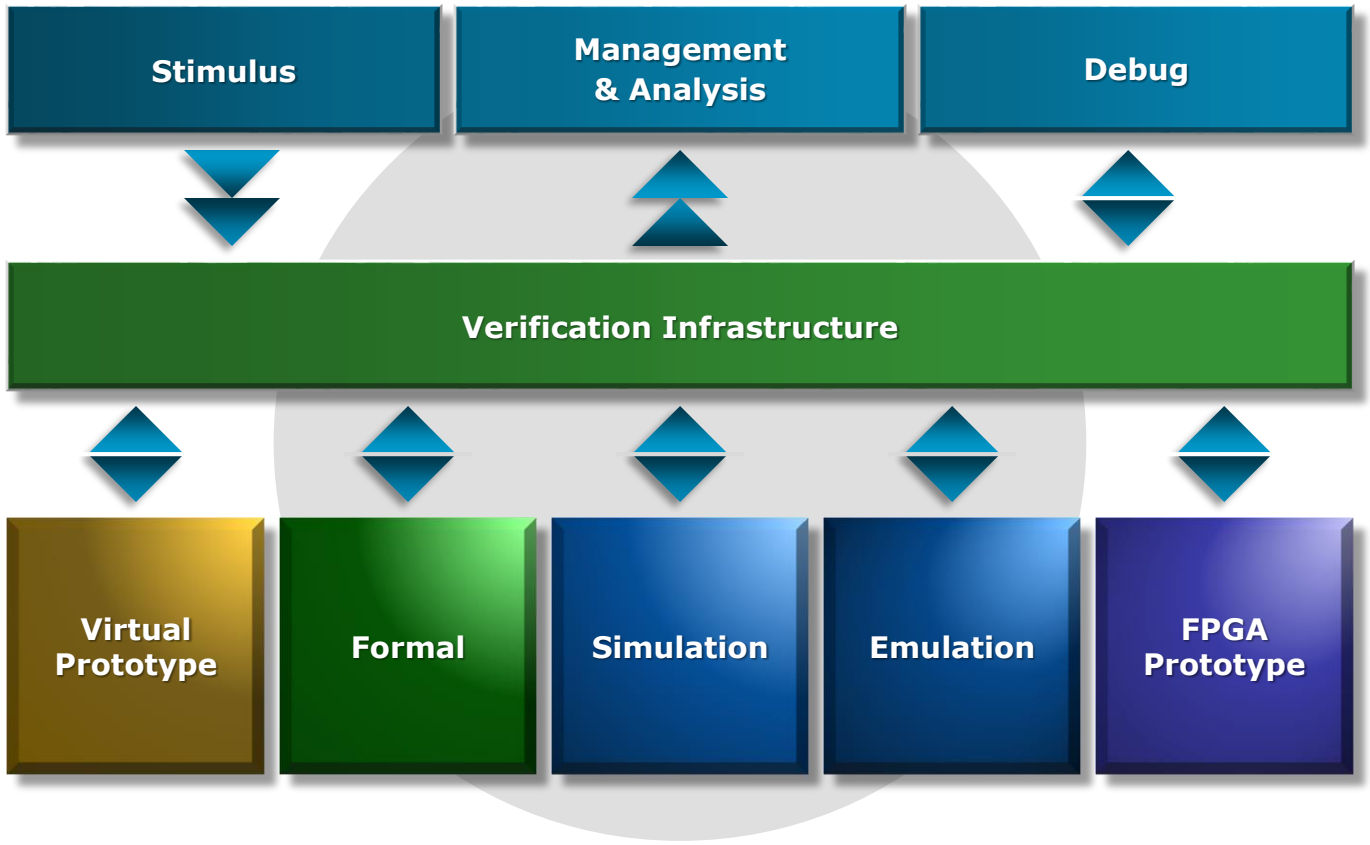
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

MENTOR EVP PLATFORM

Mentor Graphics Enterprise Verification Platform

Investing in Next-Generation Verification – Faster, Smarter, & Stronger

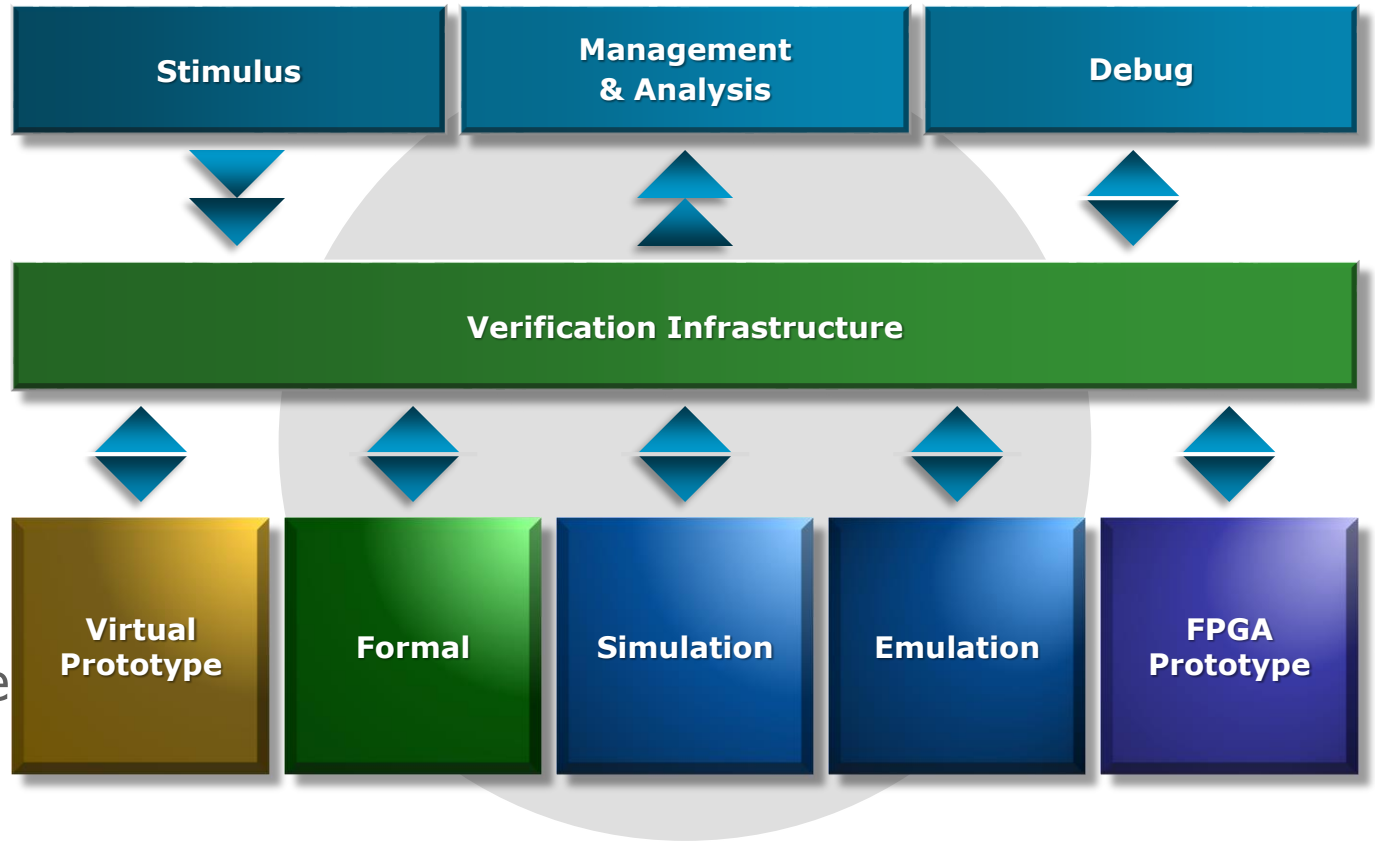
- Faster Verification
  - Virtual Prototyping
  - Formal Verification
  - Simulation
  - Emulation
  - FPGA Prototyping
- Smarter Verification
  - Stimulus
  - Metrics
  - Analysis
  - Debug
- Stronger Verification
  - Standards
  - Methodology
  - Verification IP
  - Low Power



Mentor Graphics Enterprise Verification Platform

Investing in Next-Generation Verification – The Whole is Greater than the Sum of the Parts

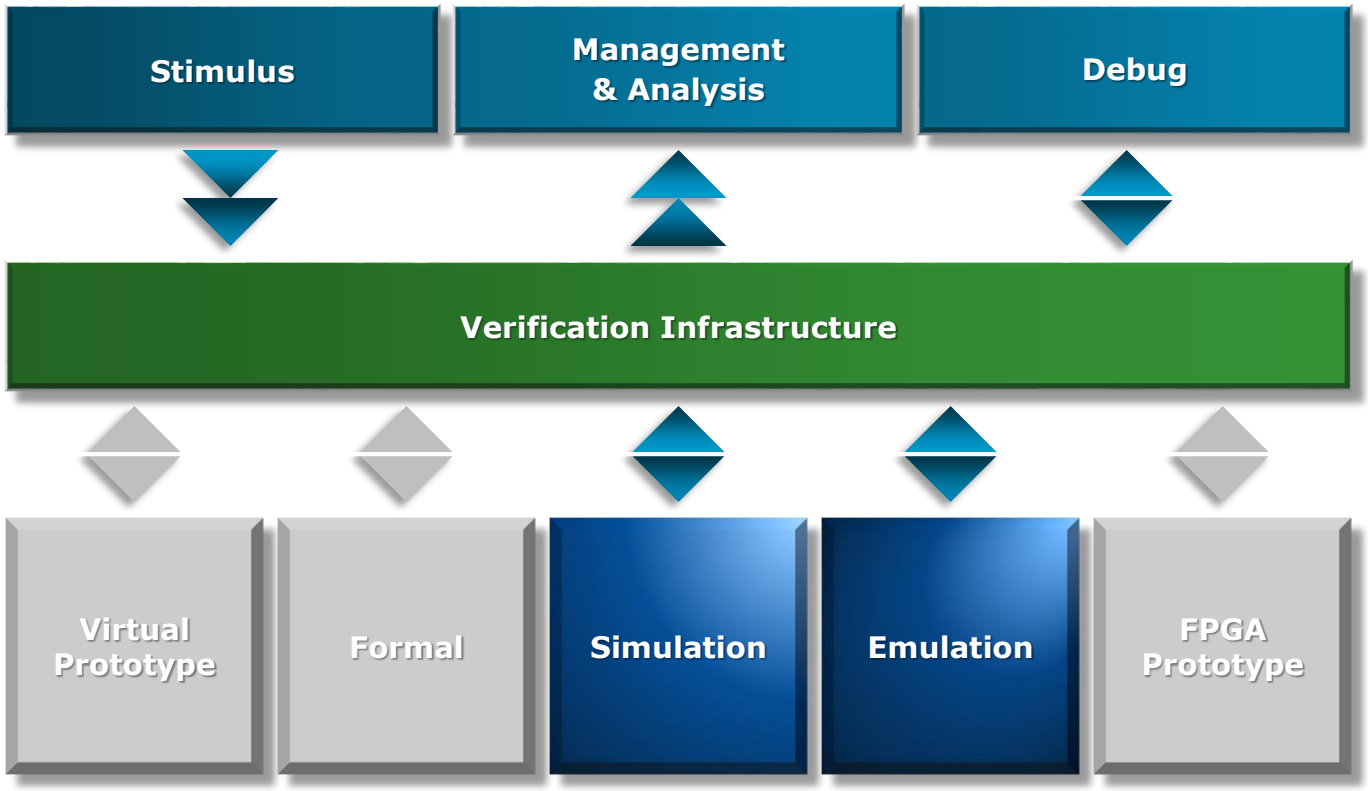
- Verification Engines
  - Interoperable
  - Shared Data
  - Globally Resourced
  - Formal Automation
- Verification Tools & Technology
  - Usable across design scope
  - Usable across engines
  - Common user presentation
- Verification Infrastructure
  - Architected and built on standards
  - Consistent VIP across engines
  - Consistent VIP across design scope
  - System wide low power flow



Faster – Accelerating Simulation via Emulation

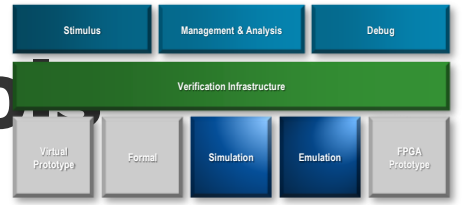
Verification Engineers Can Quickly Transition Between Questa and Veloce

- Commonality & Consistency
  - Environment
  - Methodology
  - Tools
- Interface Solutions
  - Physical Devices
  - Transactors
  - Virtual Devices
- Global Resourcing
  - Network Accessibility
  - Multi-Site
  - Multi-User

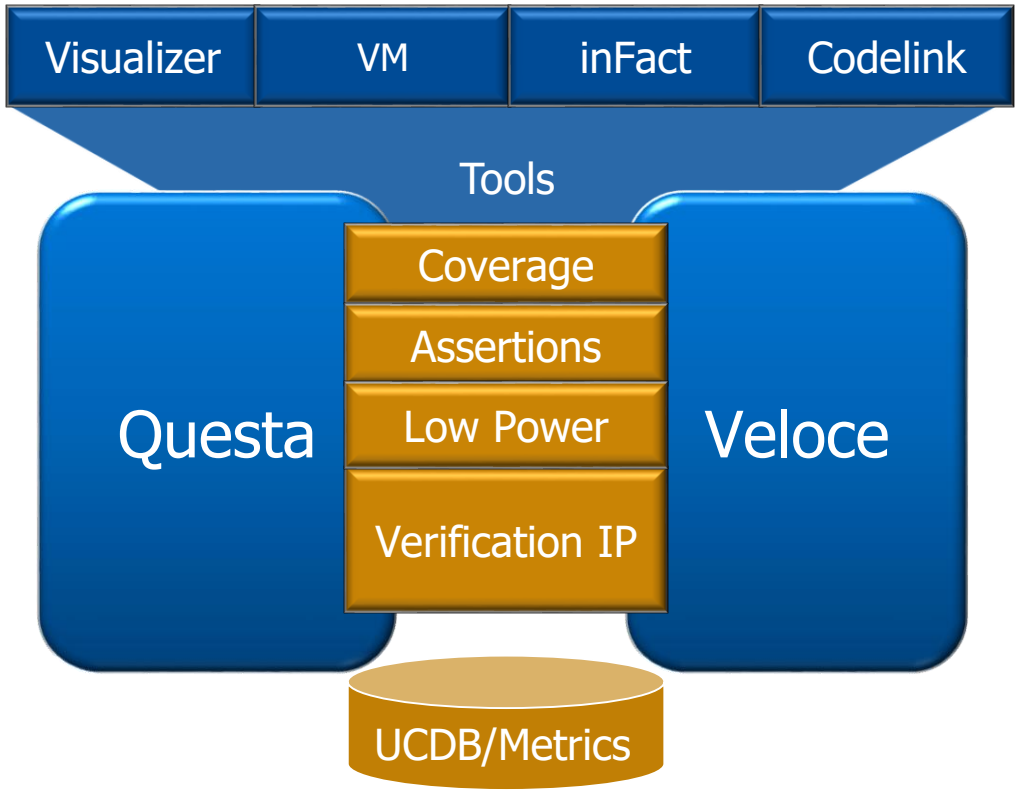


Common Environment, Methodology, & Tools

Coverage, Assertions, Low Power Verification, Verification IP, and Metrics

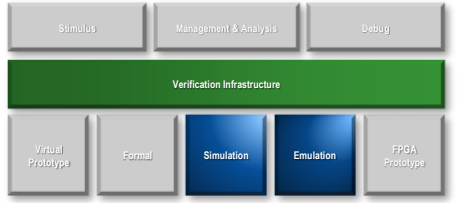


- Common Verification Environment
  - Coverage Models
  - Assertions & Checks
  - Verification IP Transactors
- Common Verification Methodology
  - Low Power Analysis Throughout
  - Single Results Database
  - Collective Metrics & Management
- Common Verification Tools
  - Visualizer Debugging
  - Verification Management
  - inFact Stimulus
  - Codelink Debugging

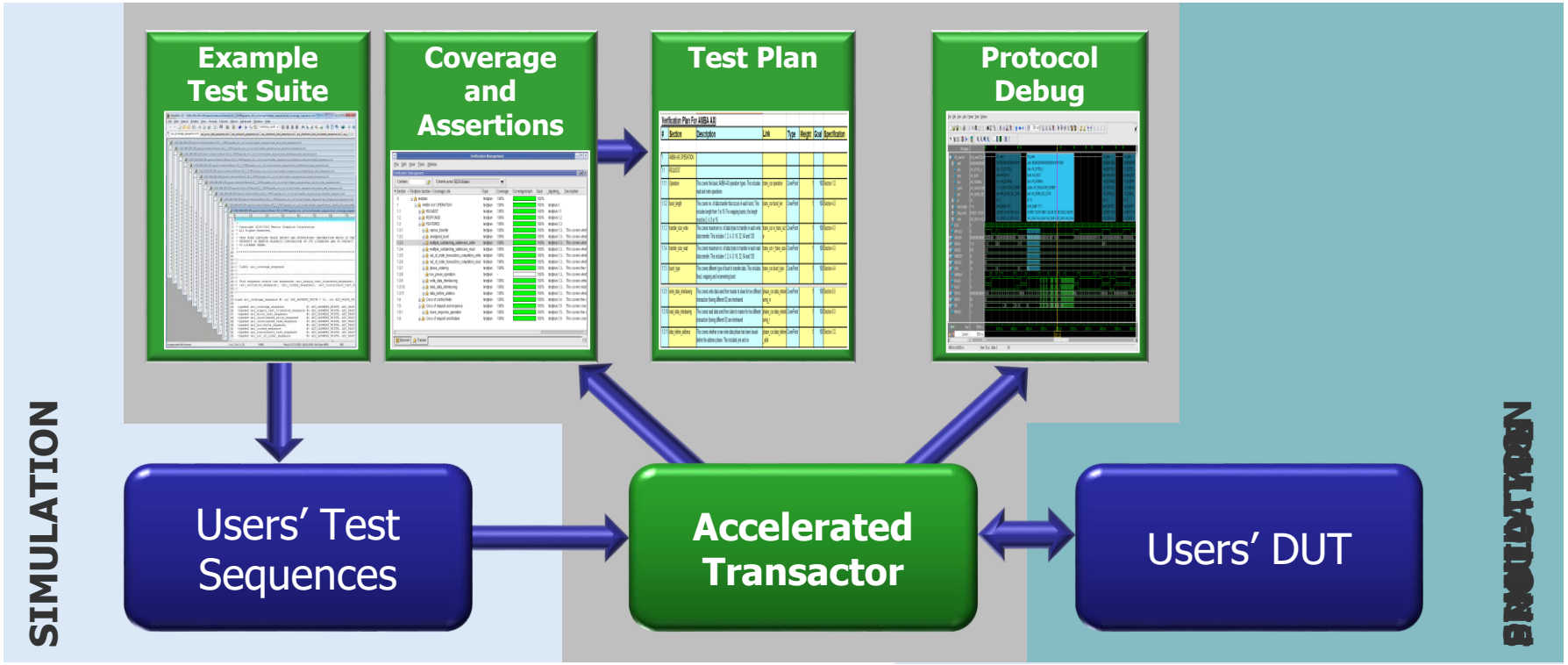


Questa Verification IP

Native UVM – Complete Models Enable Portability & Maximize Re-Use



- Portability
  - Simulation
  - Emulation
  - Prototyping
- Commonality
  - User testbench
  - DUT interface
- Virtualization
  - Emulation
  - Prototyping



Mentor® A Siemens Business

VELOCE
EXECUTIVE UPDATE

Investing in Increasing R&D Headcount

IC Verification

+31% R&D Headcount

+ Acquisition of Solido
+ Acquisition of Austemper

Mentor Emulation

+33% R&D Headcount

+ Acquisition of Sarokal

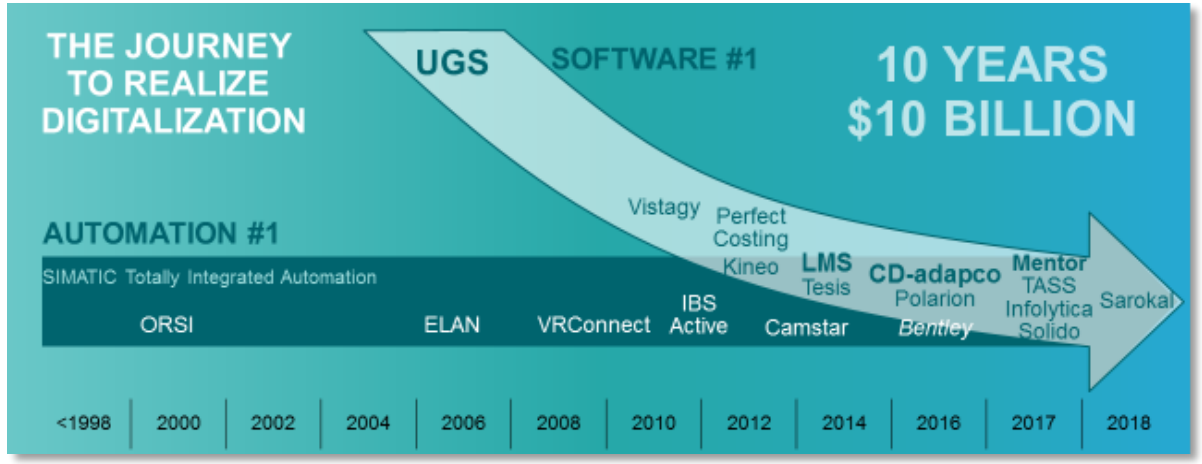
> Siemens agreed to acquire Mentor for $4.5 billion and we would not make such a significant investment to short change Mentor's strengths in IC and SoC design.
>
> The world of IC and SoC design will be new to us, no doubt about it. However, it is not new to Mentor, and that's why we are so interested not only in Mentor's flagship products but also the talented people that will come with the acquisition.
>
> Mentor is truly focused on providing the best technology. Siemens is excited to make future investments in Mentor's key EDA technologies so that those can grow even faster.

Chuck Grindstaff
Executive Chairman
Siemens PLM

Tony Hemmelgarn
CEO, Siemens PLM

The Bigger Picture for Mentor + Siemens

Electronics are now at the Heart of all Systems



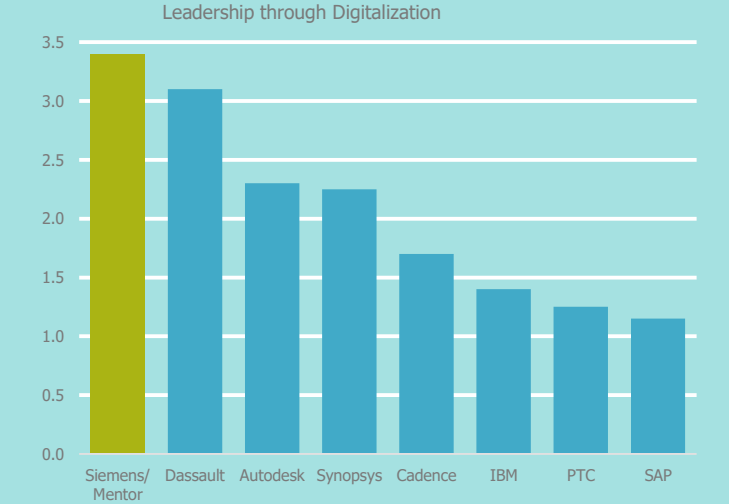
Creating the Software Leader for the Product Lifecycle

Mentor+Siemens is taking our Customer relationship/partnership to a different level

Now the Leader in Industrial Software for Digital Innovation

"Digital Twin"

#1

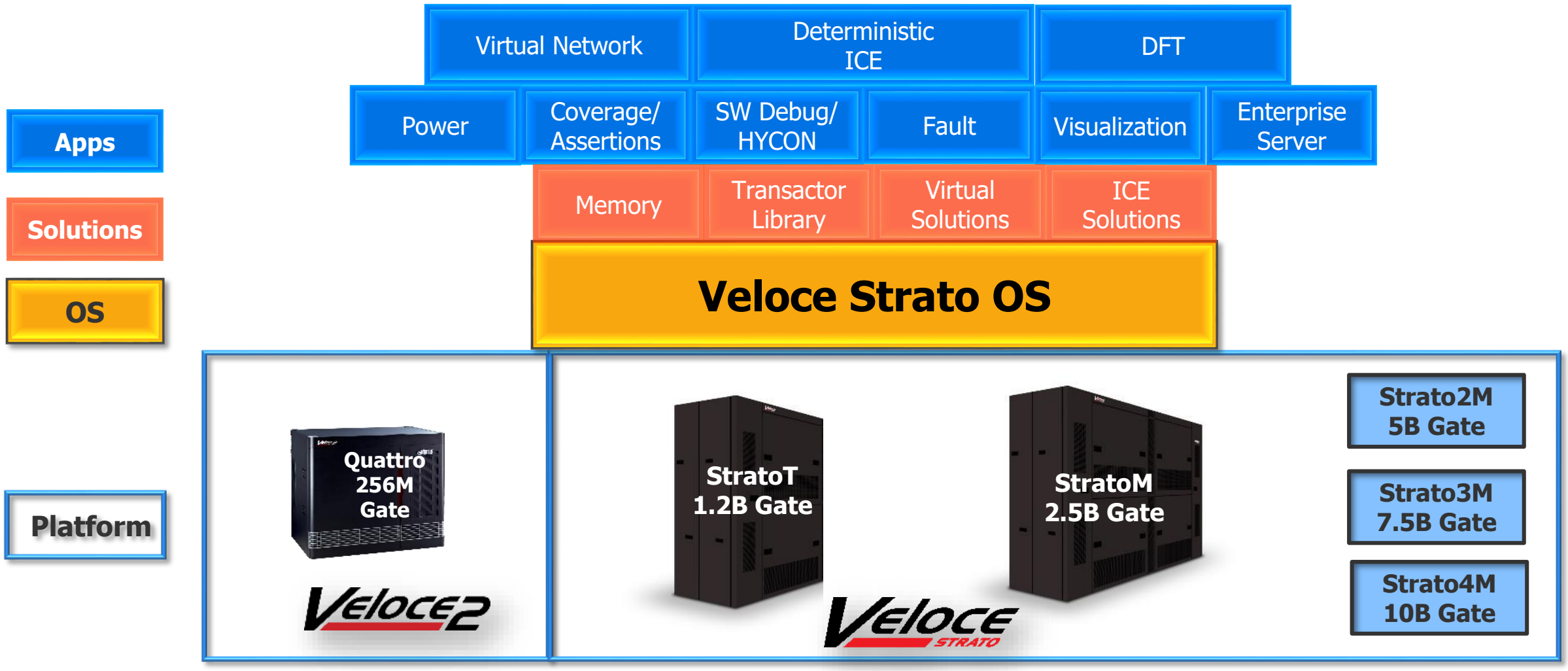


Mentor® A Siemens Business

VELOCE
PLATFORM OVERVIEW

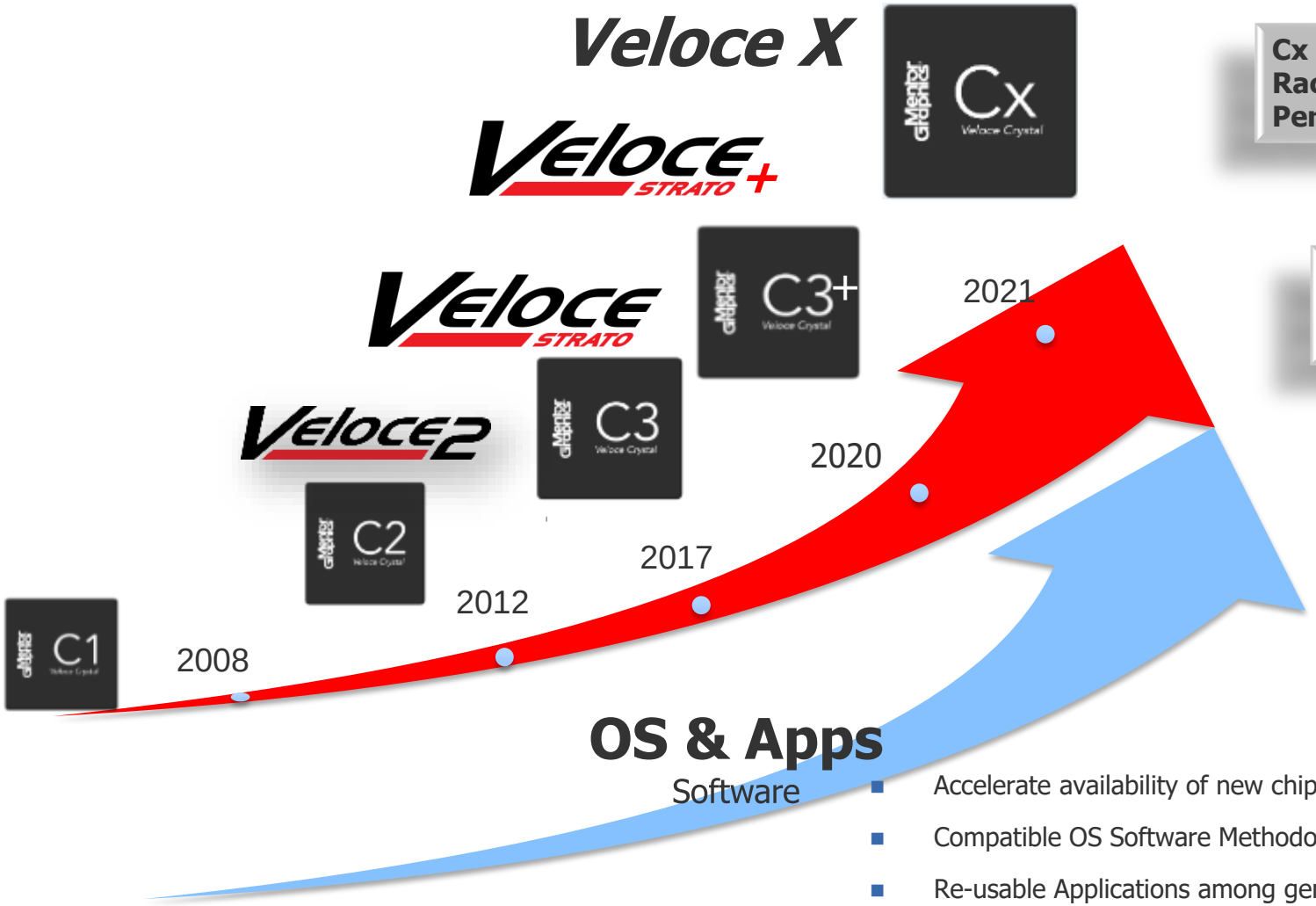
Veloce the Complete Verification Platform

ISO 26262

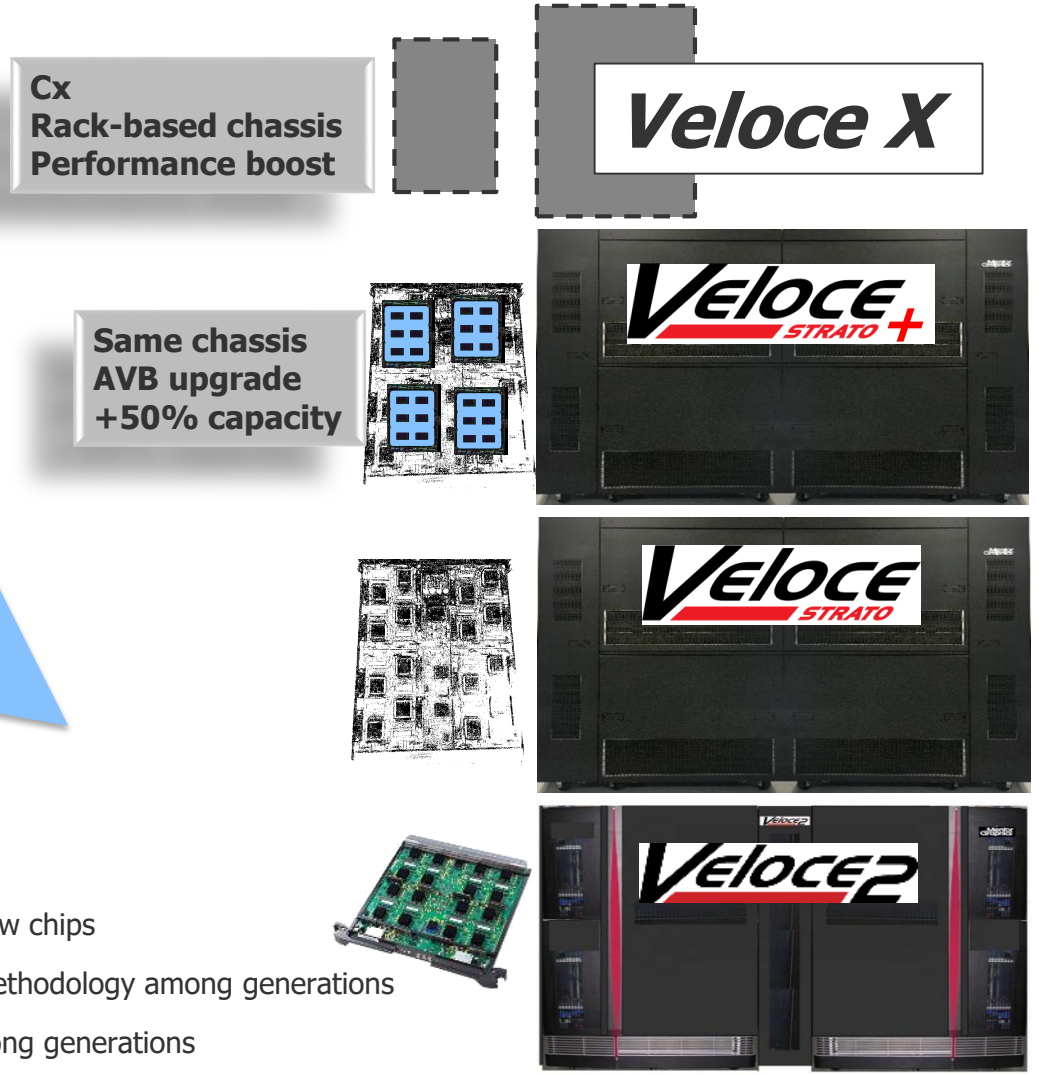


Mentor A Siemens Business

Funded Custom Chip and HW Roadmap



- Accelerate availability of new chips
- Compatible OS Software Methodology among generations
- Re-usable Applications among generations
- Re-usable Veloce Solutions



Veloce Strato: Value Proposition

Capacity Scaling
(40 MG => up to 15 BG)

5x Productivity
(3x Compile, 3x Bandwidth, 10x Wave Upload)

Data Center Friendly
(Footprint, Air Cool, 1/3 Power/Gate, Uptime/Service)

Easy Adoption, Migration and Use
(Same Scripts, Apps, Use Model, Flows & Resource Efficient)

Quality
(Reliable, Robust, Resilient)

Veloce Strato Hardware Platform

StratoM

StratoM Memory

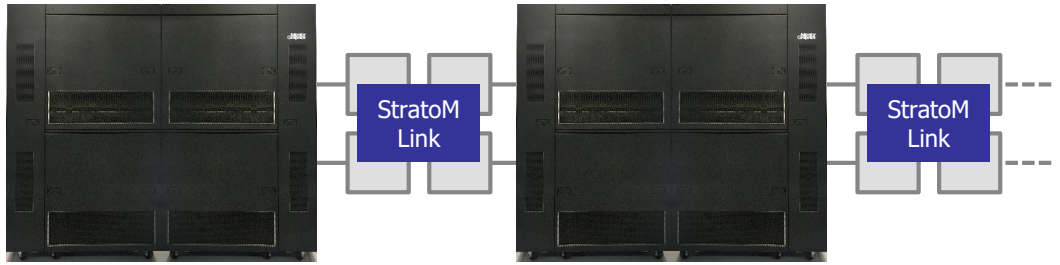
Chip Memory	**33 GB**
Board Memory	**128 GB**

Capacity	Performance	Power Consumption	Users
Up to 2.5 BG	1+ MHz	Up to 35 kW (air cooled)	Up to 64

StratoT

Capacity	Performance	Power Consumption	Users
Up to 1.2 BG	1+ MHz	Up to 17 kW (air cooled)	Up to 32

Path to higher capacity



10 BG, 15BG

Veloce Strato: Flexible and Scalable Capacity

Veloce StratoT

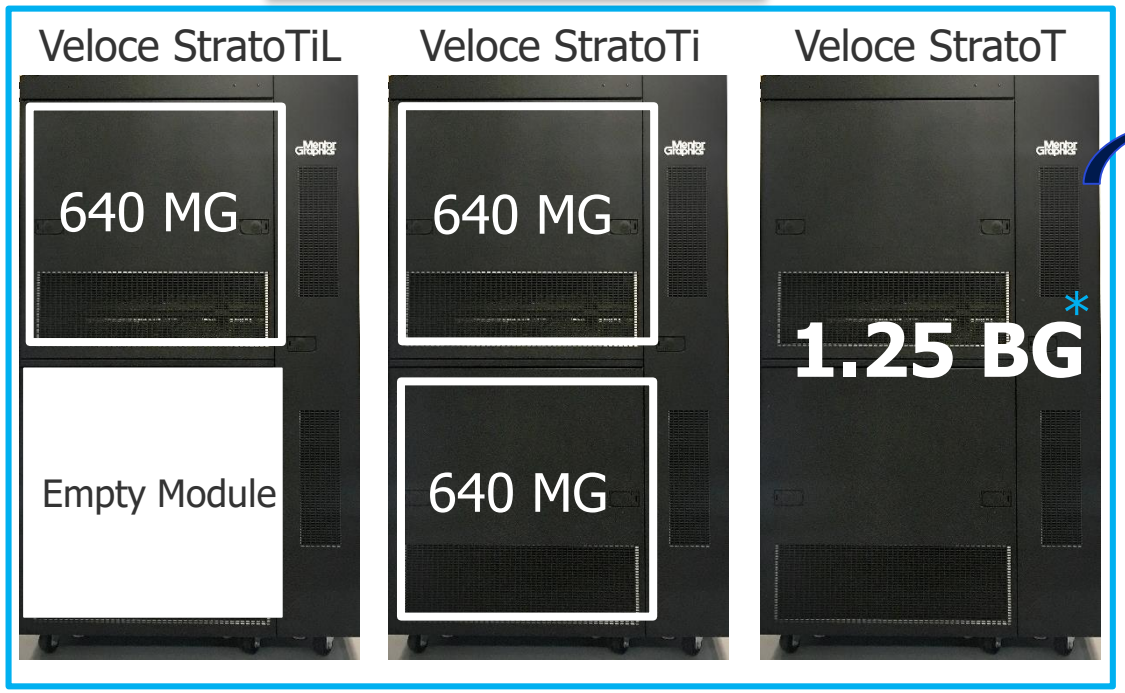
Veloce StratoM

Veloce Strato2M

No Impact on Performance and Gate utilization as Design size grow

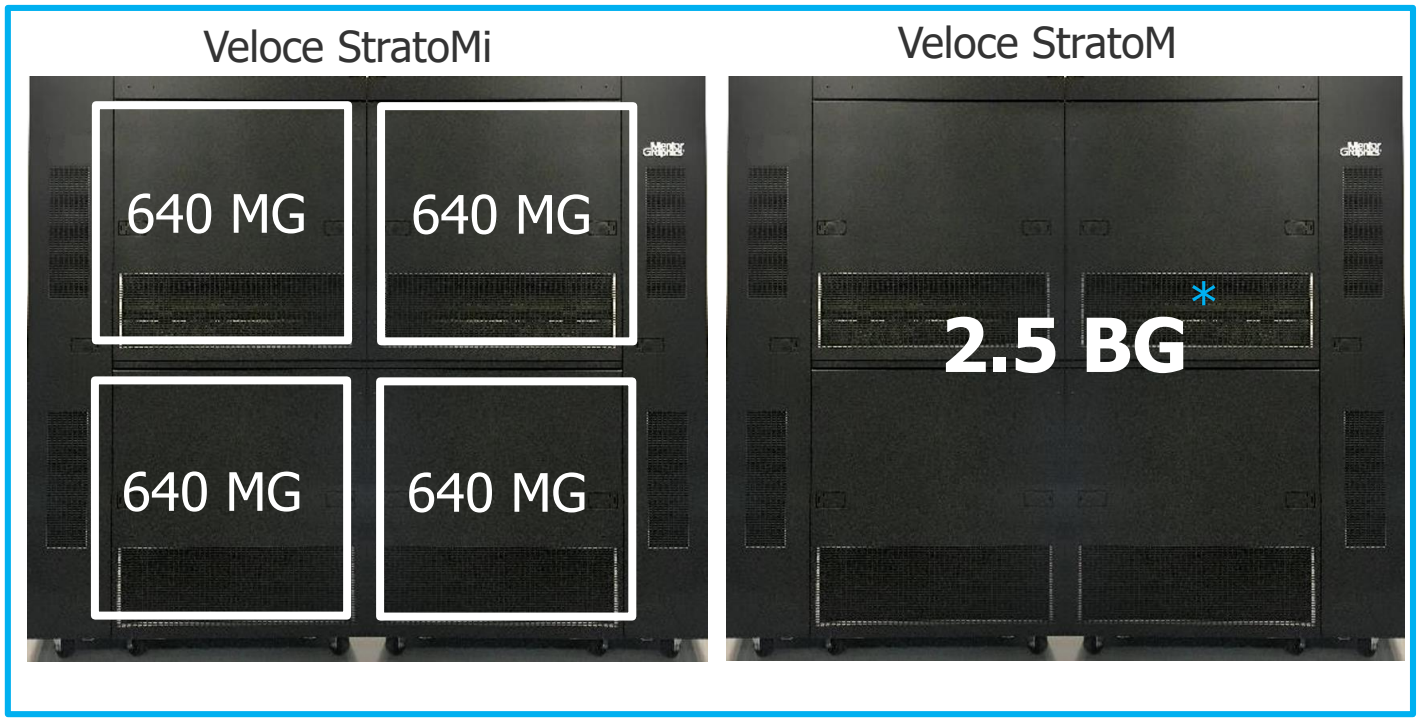
Chassis Options: Flexible and Scalable Capacity

Veloce StratoT Family



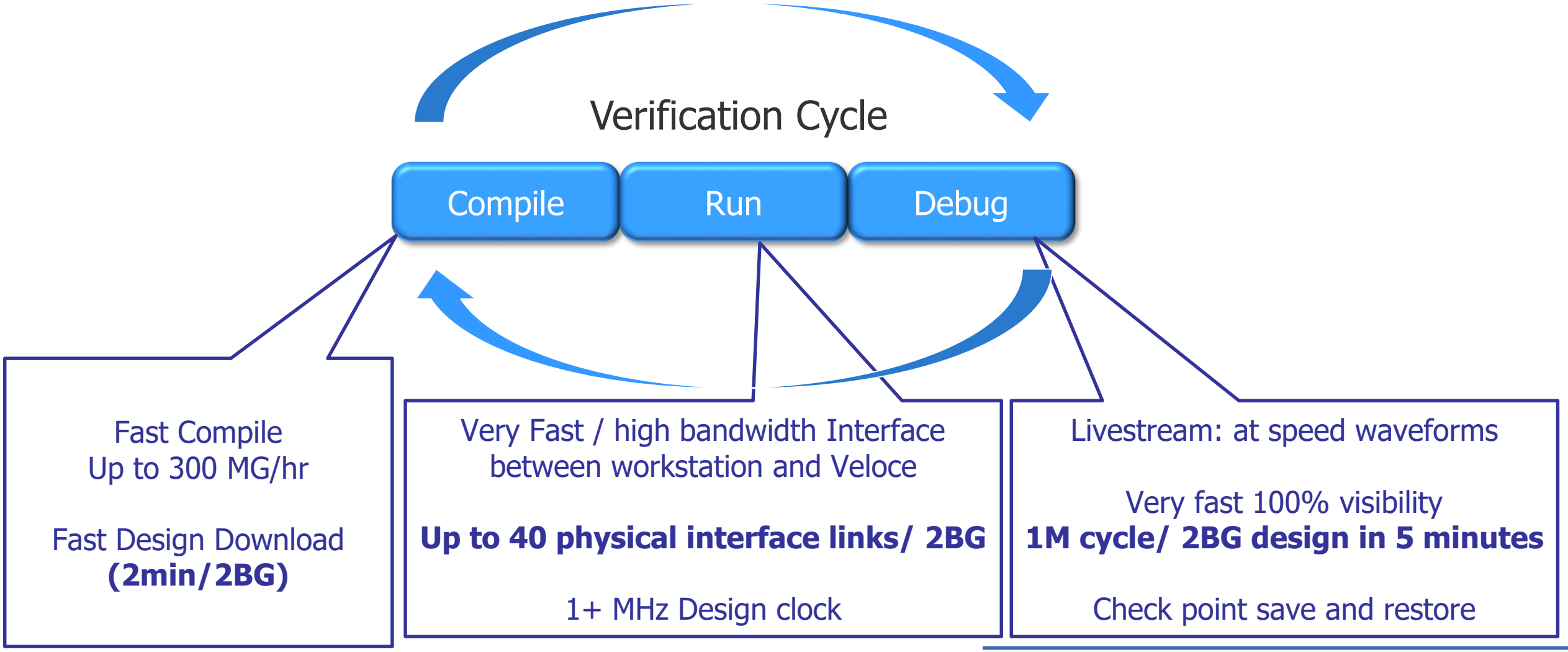
Veloce StratoT2M

Veloce StratoM Family



***Veloce gates, utilization is around 80% depending on design**

Improves Verification Productivity



Fully Automated and Unified Compile

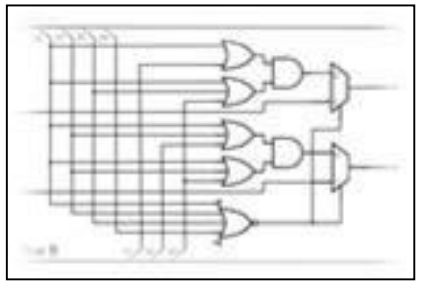
RTL Design

```
module ddr1_core (DOUT, DIN, WA, RA, WE);
    input [23 : 0] WA, RA;
    input [7 : 0] DIN;
    input WE;
    output [7 : 0] DOUT;
    reg [7 : 0] DOUT;
    reg [7 : 0] mem [16777215 : 0];

    always @ (posedge WE)
    begin
        mem[WA] = DIN;
    end

    always @ (RA)
    begin
        DOUT = mem[RA];
    end
endmodule
```

Compiler



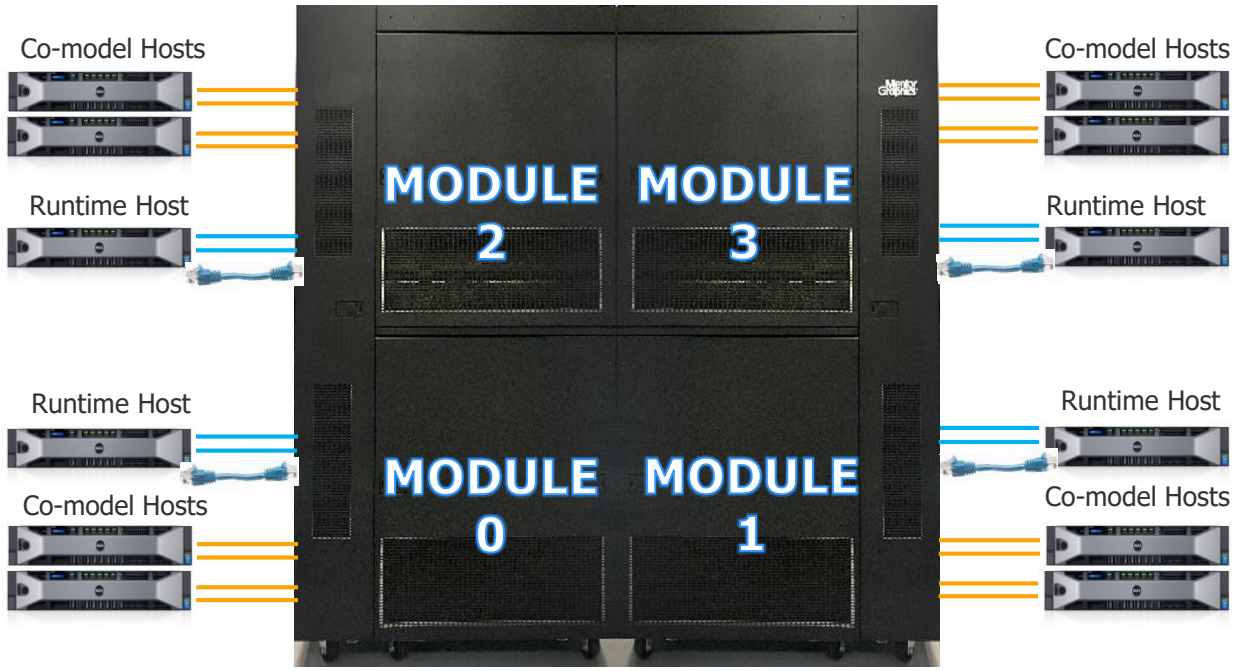
Compiler

Crystal SoC

Unified Compilation Flow for ICE, Acceleration, Virtual and Hybrid Runtime Selection to enable ICE or Virtual

300 MG per hour Today for Highly Repetitive Designs

Fast and High bandwidth Channels

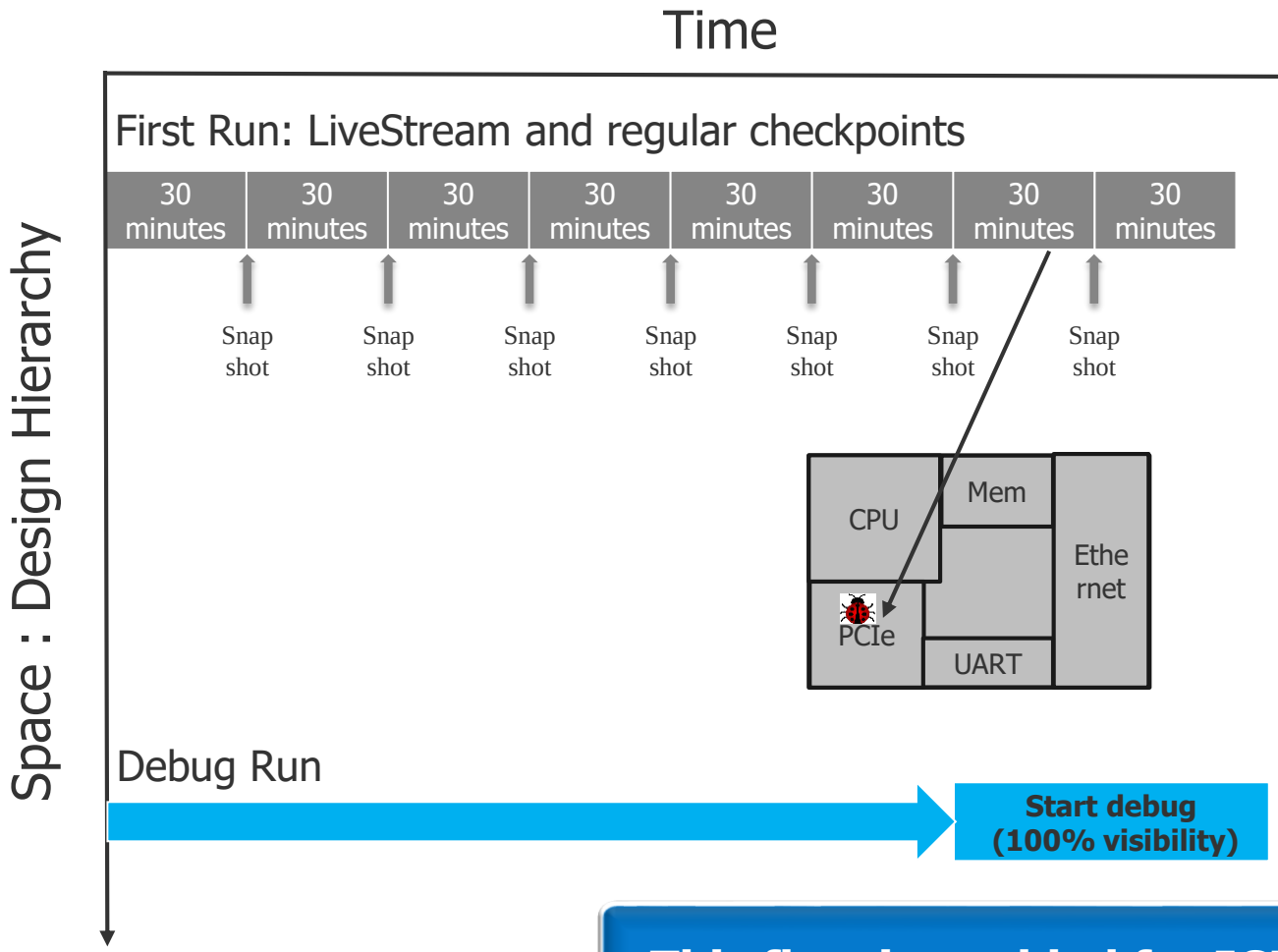


- Optical technology with latest PCIe protocol
  - Optimized data packing and transfer
  - 40 physical links / StratoM
  - 64 parallel users

- User Benefits
  - Time to Debug
  - Time to Power
  - Design and memory download
  - Testbench acceleration (UVM/SC/C++)
  - Native Support C, SystemC, C++
  - High bandwidth for Virtual environments
  - Efficient Debug for ICE Environments

VELOCE USE MODE

Highest Debug Productivity
LiveStream & Check Point Save and Restore

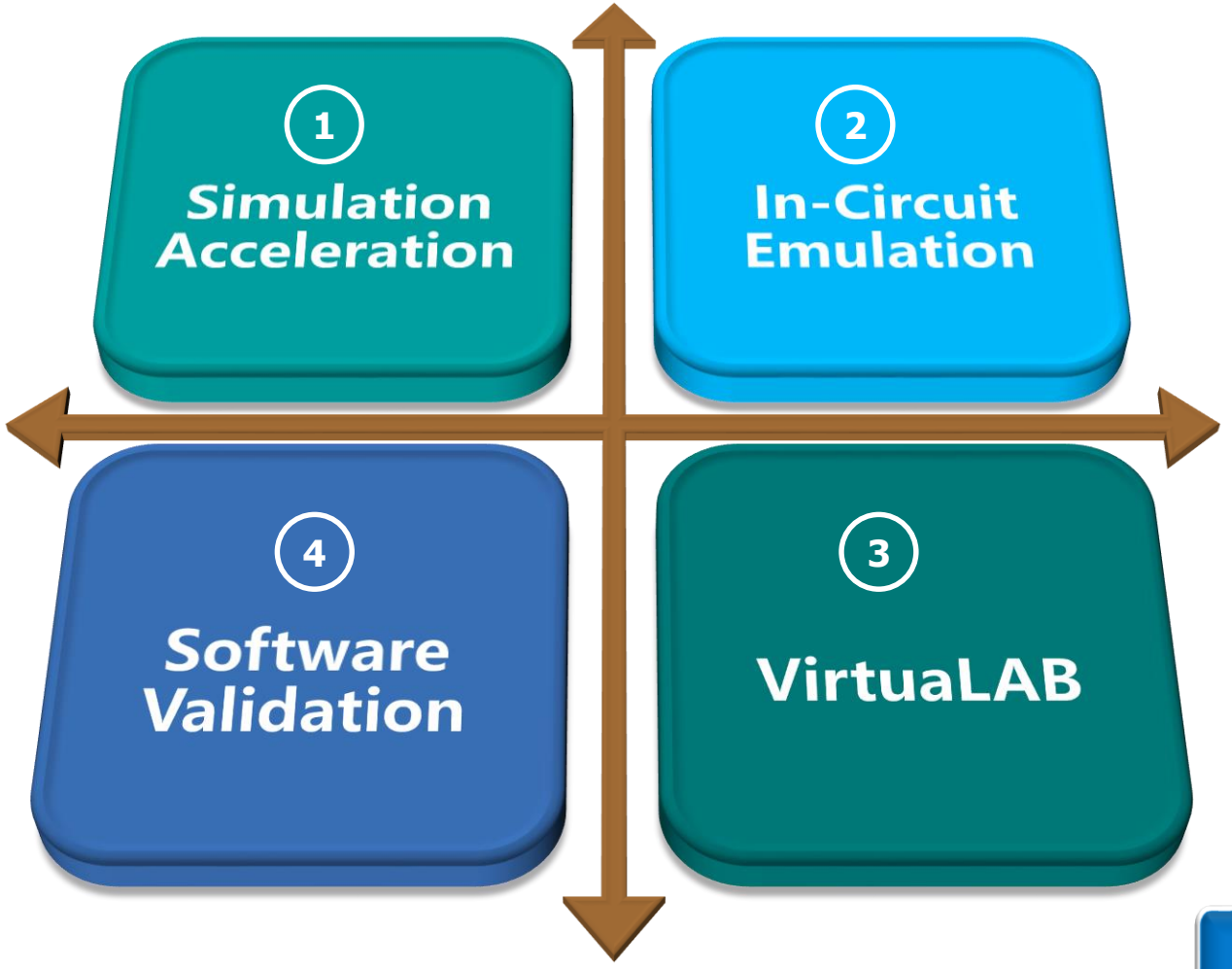


- First run
  - LiveStream: run emulation at full speed
  - Marching waveform (selected signals) for entire test duration
  - Chip performance analysis
  - Take regular checkpoints
- Debug run
  - Fast forward to the nearest checkpoint
  - Enable full debug: Assertions, Triggers, Waveforms, Monitors

This flow is enabled for ICE, Acceleration, Virtual and Hybrid

Pre Silicon
Post Silicon

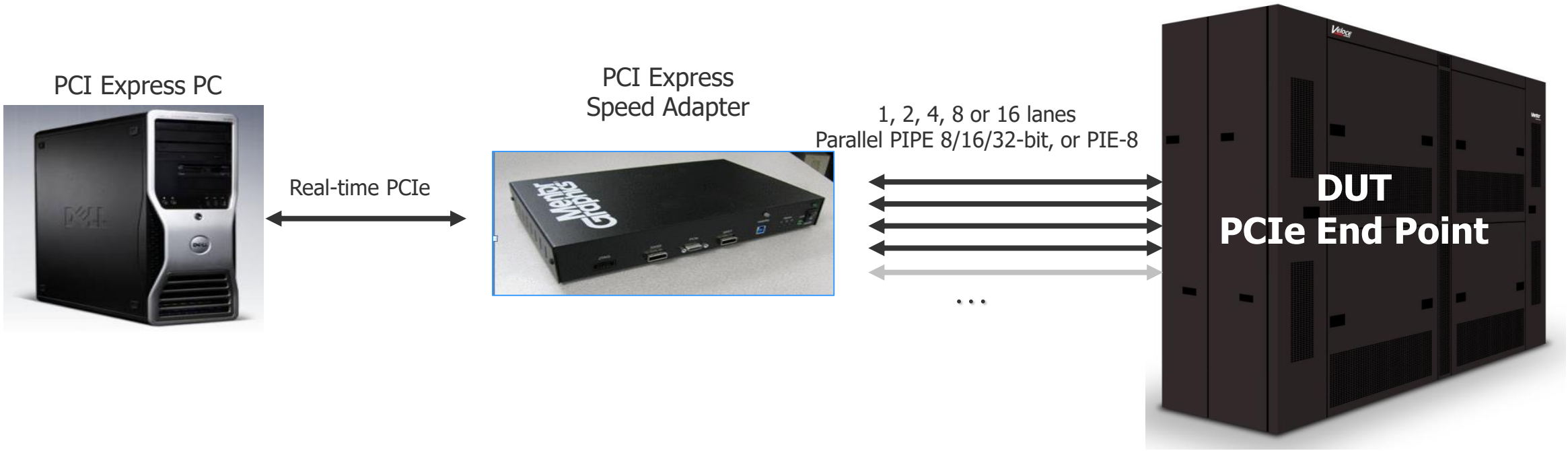
Complete Solution for All Verification Use Modes



1. SW test benches
   - UVM/SV
   - SC/C++
2. Apply stimulus using real devices
3. (NO test benches)
   - Physical devices (ICE)
   - Virtual devices
4. SW validation

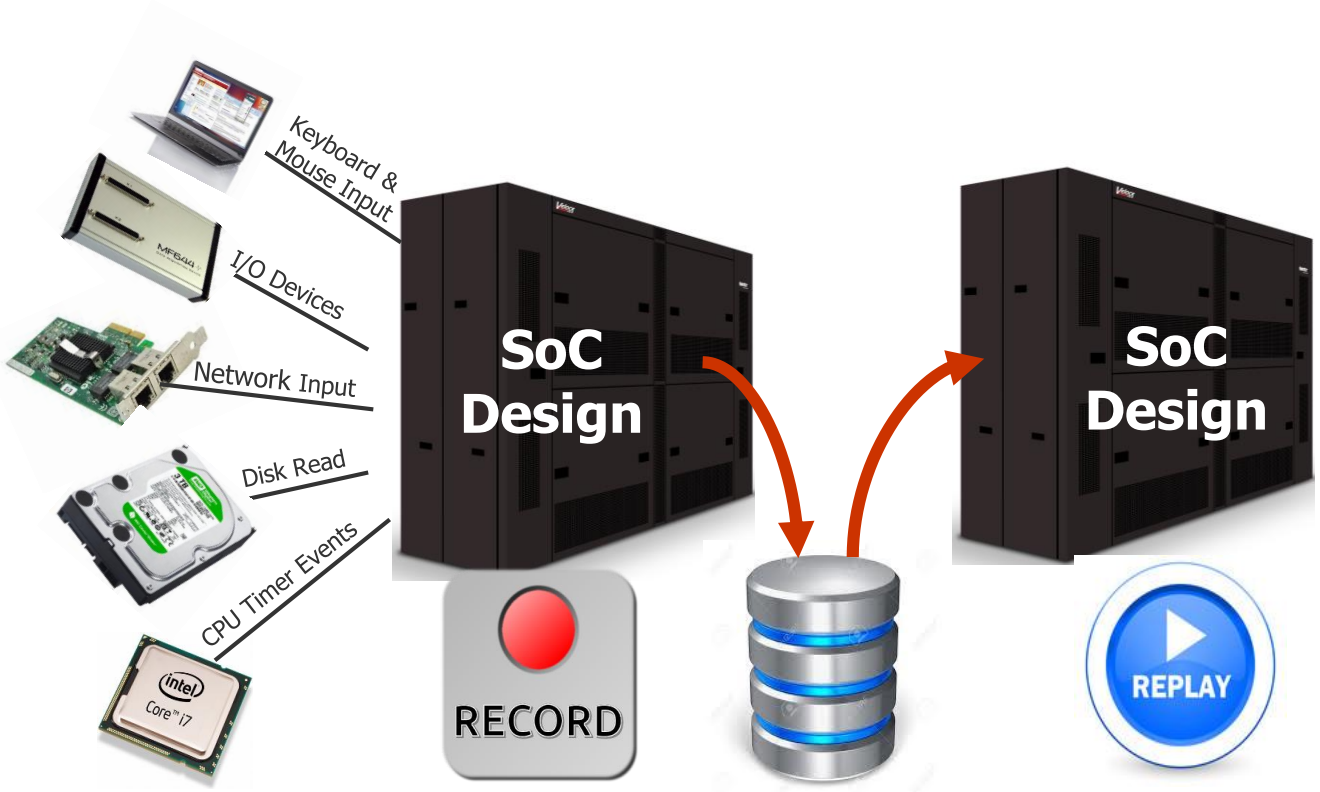
Complete end to end SoC Verification/Validation

Veloce ICE Use Mode : PCIe example



Mentor provides speed bridges for all standard protocols

Veloce Deterministic ICE App

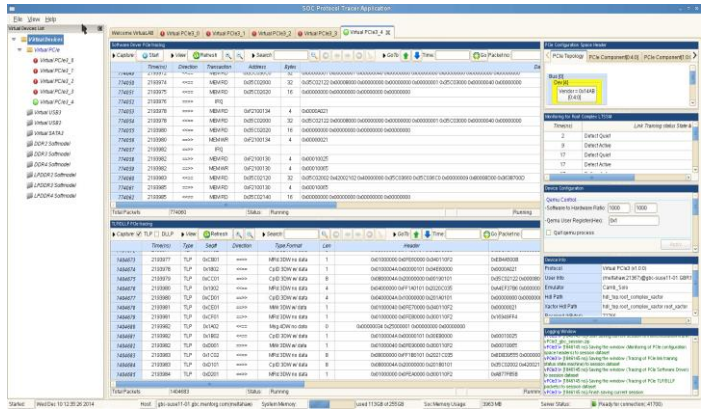


- Delivers repeatable behavior for ICE debug
- LiveStream generates waveform for entire ICE run
- Apps: Power, Coverage, …

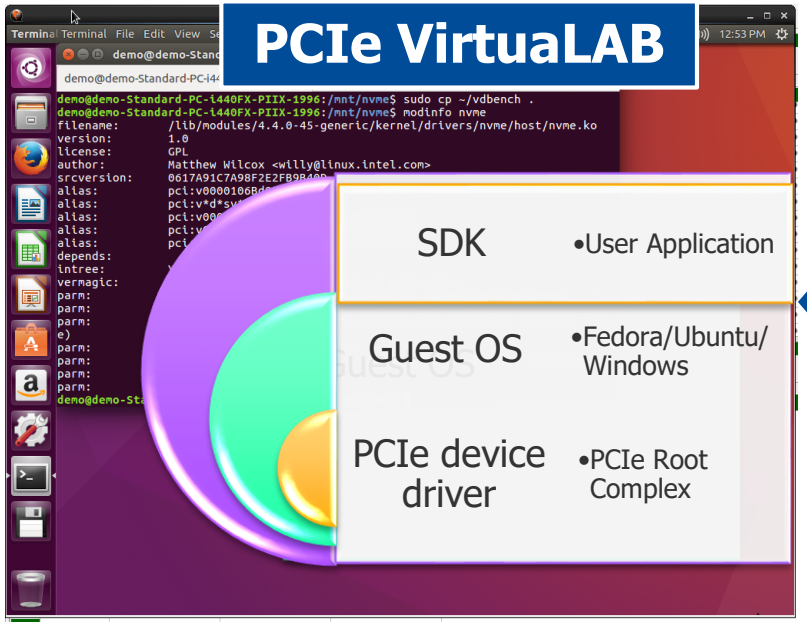
Boost productivity for the traditional ICE use mode
Strengthen ICE offering and enable path from ICE to Virtual

Veloce VirtuaLAB : PCIe

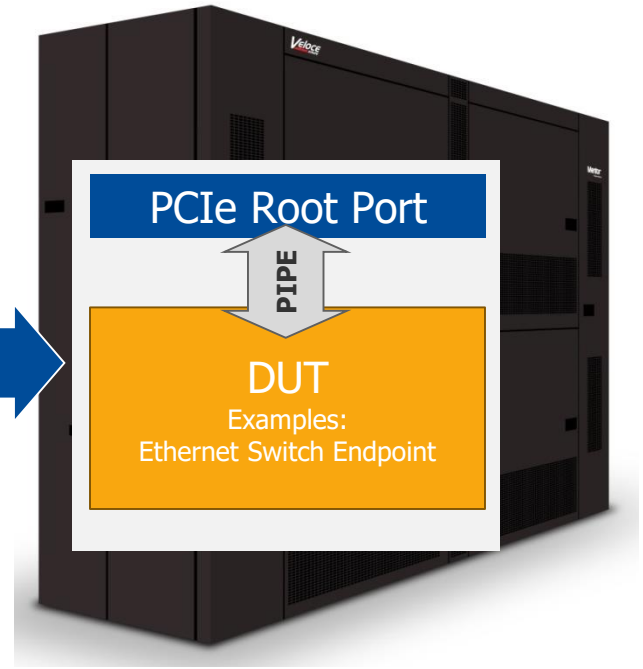
- Same functionality as ICE with higher productivity and flexible/ easier debug
- SW validation / native SDK
- Accurate performance analysis (bandwidth and latency measurements)
- Protocol analyzer
- Checkpoint save restore after the initialization



Protocol Analyzer

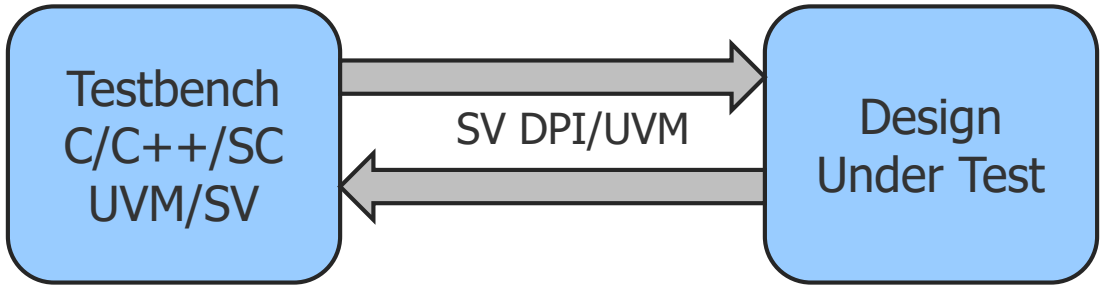


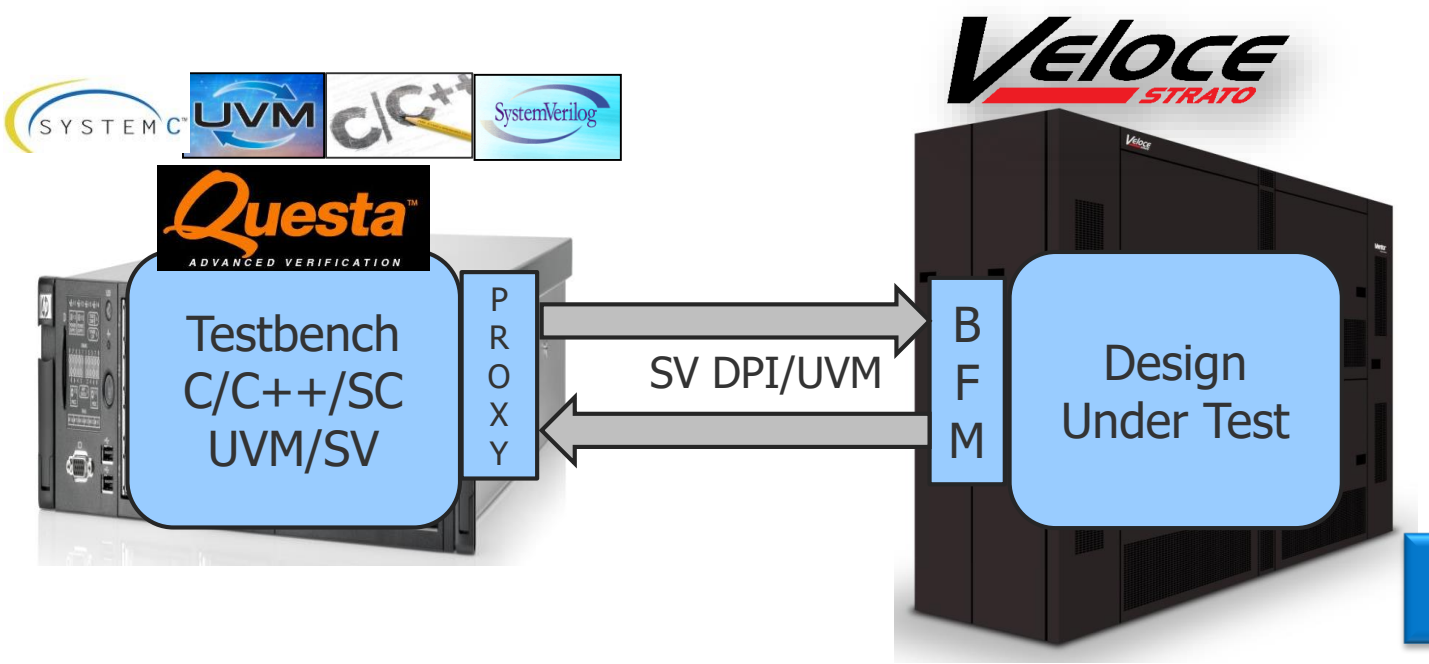
Co-Model



VirtuaLAB: A Differentiated offering from Mentor

Accelerating Simulation-Based Verification





Ease of Bring-Up

Design

- **Support modport expressions, 2015 SV constructs, …**
- **Expanding $display, $fscanf, $random, $readmemh support ….**

Testbench

- **Support for #delays**
- **Hierarchical access to RTL signals and clocks**
- **Performance profile report**

Behavioral Constructs Supported by Veloce

- RTL subset
- SystemVerilog interface
- SystemVerilog Virtual Interface
- SystemVerilog final block
- SVA sampling functions ($rose, $fell, $past, $stable, $changed, $sampled)
- SVA functions $countones, $onehot, $onehot0, $isunknown
- Language based force/release
- C-API based force/release
- $testplusargs and $valueplusargs
- Initial blocks
- Behavioral clock/reset generation
- System tasks; $display, $fdisplay, $fwrite, $fscanf, $random
- DPI function/task calls
- SCE-MI 2.0 compliant transaction pipes
- Clocked tasks
- Gated clocks
- Variable delay clocks
- Multiple drivers
- Memory array
- SV cover groups
- Support for $time, $realtime
- Support for complex data-types in DPI calls
- Nested Interfaces

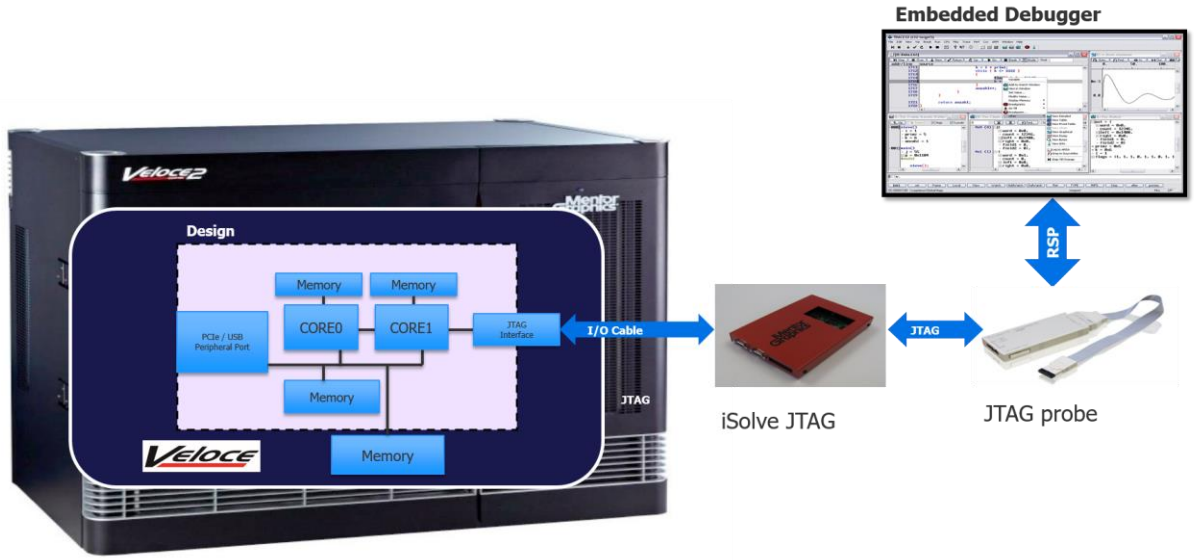
100 to 1000x Acceleration

Software Debug Solutions for Veloce

- Debug Probes
  - Traditional interactive debug using wired JTAG connection
  - Physical Probe connected to design through I/O cables
  - Enables control and visibility into software running on the processors in Veloce
- Virtual Probes
  - Traditional interactive debug using JTAG transactors
  - No physical JTAG probe needed – fully virtualized connection
  - Delivers the same capability as physical probes without the wires and hardware
- Codelink
  - Off-line post emulation software debug
  - Completely non-intrusive debug
  - Enables efficient sharing of emulation resource

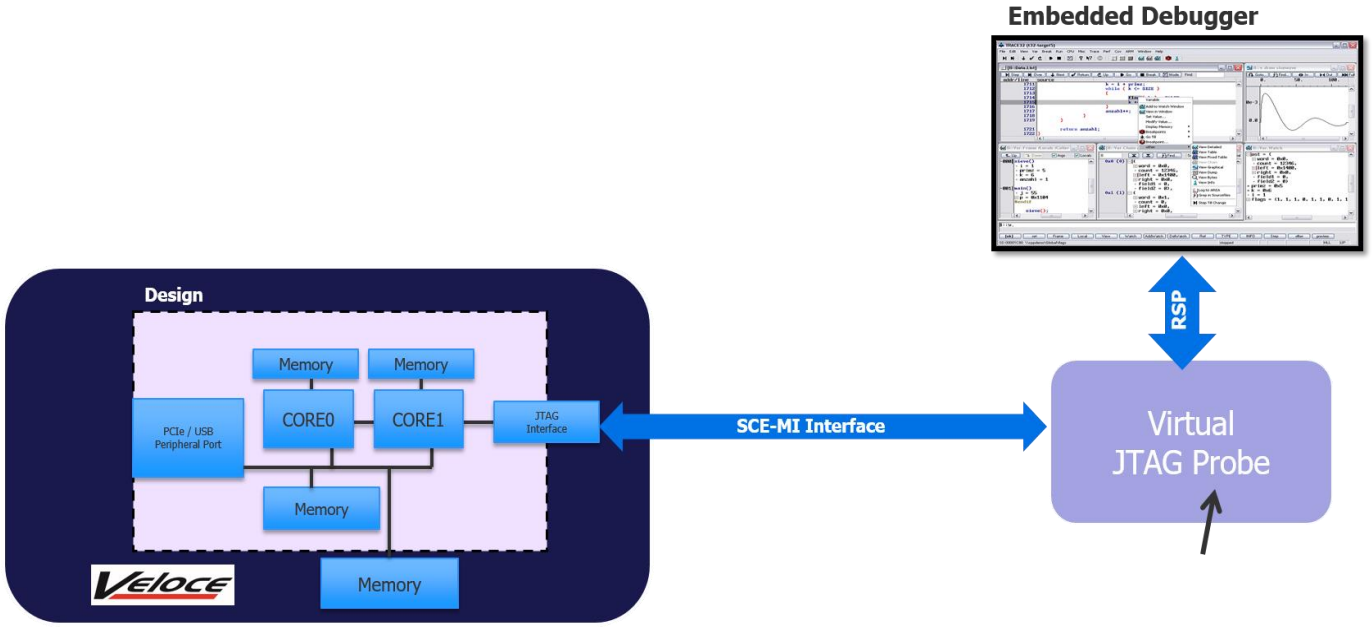
Software Debug via JTAG

- Enables software debug through traditional JTAG interface
  - Complete run control with memory and register visibility
- Interact with hardware under design
  - Peek and poke hardware registers
- Validate debug connection before tape-out
  - Exercise JTAG circuitry and Coresight logic
- Works with all JTAG probes and embedded debuggers
  - Exposes standard 20 pin DIP connector



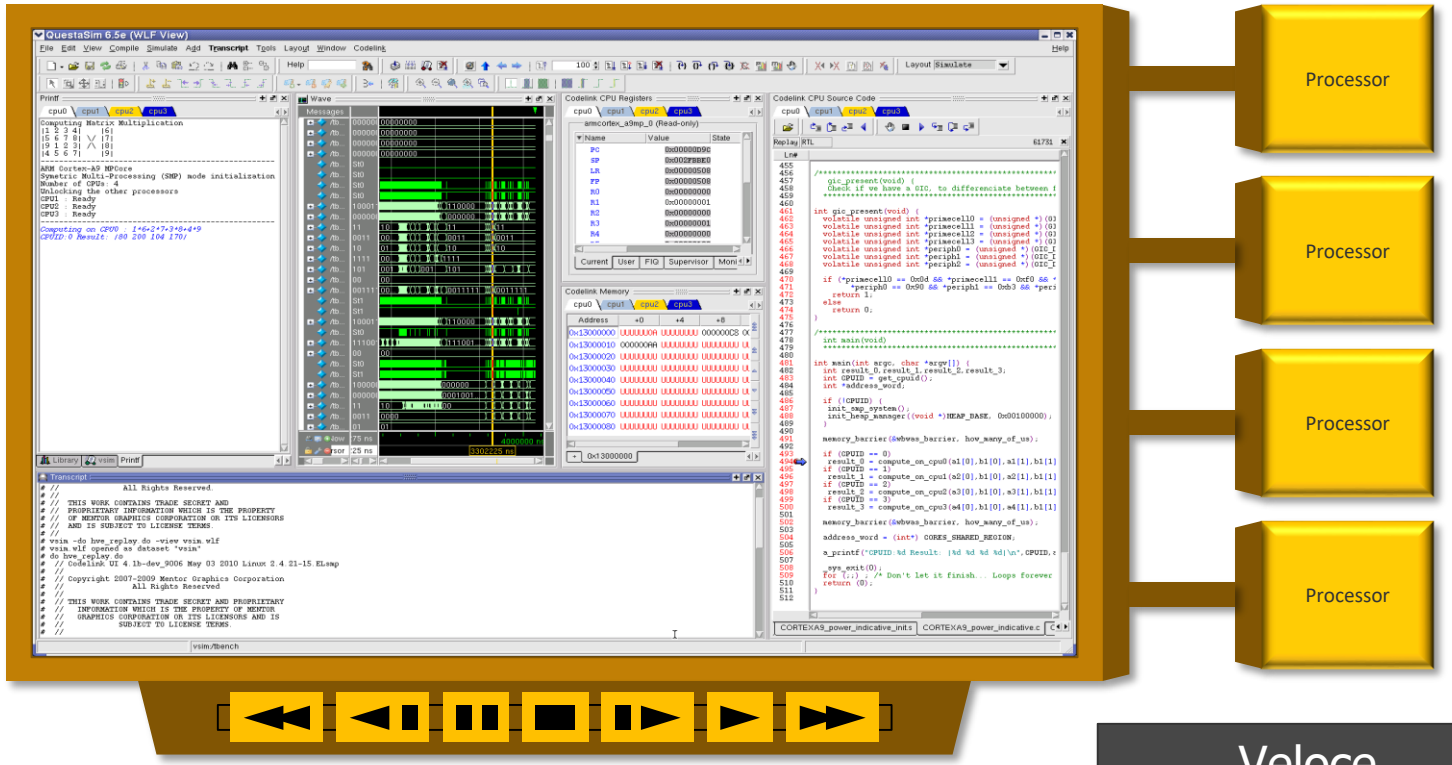
Software Debug via Virtual JTAG- Veloce Vprobe

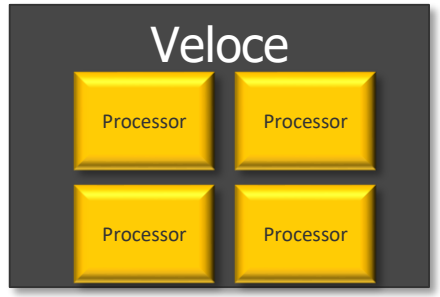
- All the capabilities of a physical JTAG connection- Equal or better performance!!
- Emulation clocks can be stopped and restarted
  - Enables time for waveform uploads
  - Debug and analyze hardware while system is stopped
- Fully compatible with TBX transactors and VirtuaLAB test bench components
- Fully supports Checkpoint and Restore
- Allows designes to freely move from one emulation resource to another
  - Not tied to a specific set of I/O Cards
- No need to maintain physical hardware



Software Debug via Veloce Codelink

- Emulation Debugging
  - Off-Line Replay
- Synchronized Viewing
  - Waveforms
  - CPU Registers
  - Memory
  - Source Code
  - Output
  - Variables
- Digital Playback System
  - Fast forward
  - Rewind
  - Single-step
  - Pause
- Runs at 50MHz





Veloce the Complete Verification Platform

ISO 26262

Apps

Solutions

OS

Platform

Virtual Network | Deterministic ICE | DFT

Power | Coverage/ Assertions | SW Debug/ HYCON | Fault | Visualization | Enterprise Server

Memory | Transactor Library | Virtual Solutions | ICE Solutions

Veloce Strato OS

Veloce2

Veloce STRATO

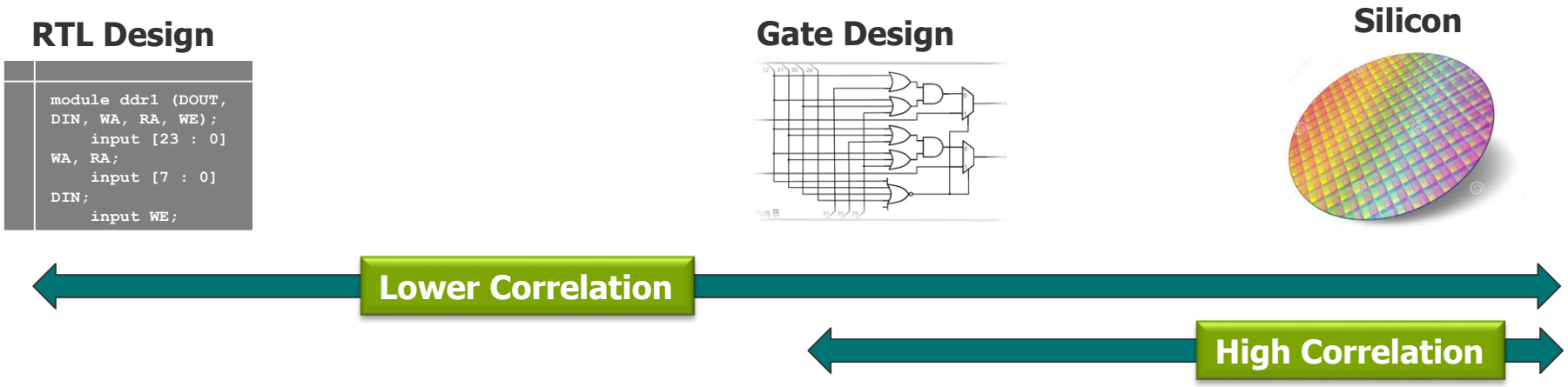
Strato2M 5B Gate

Strato3M 7.5B Gate

Strato4M 10B Gate

Mentor A Siemens Business

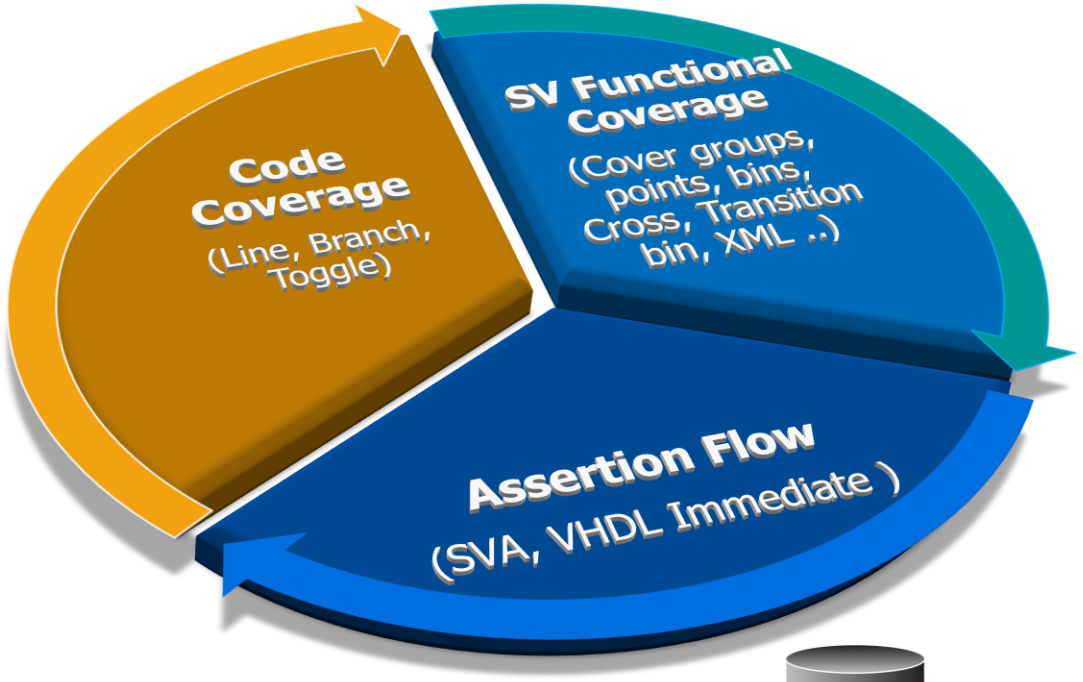
Enhanced Veloce Gate Level Flow



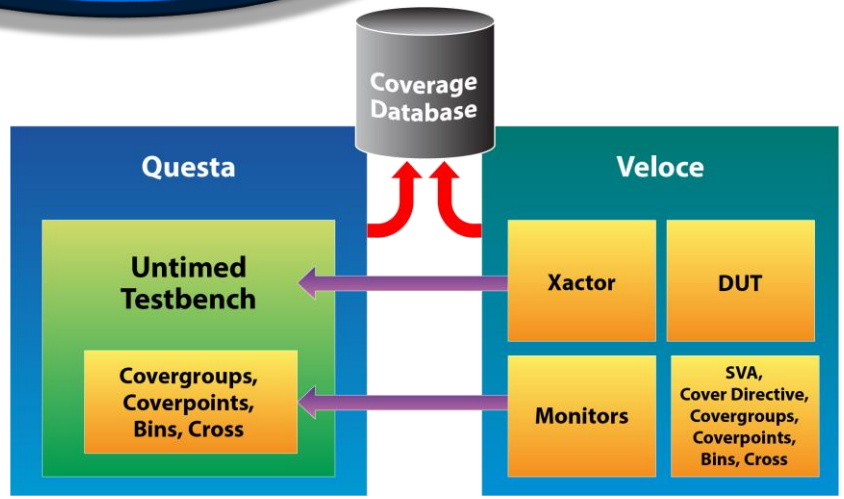
- Gate level design
  - Accurate representation of Silicon
  - Gate verification a big value (GLE, Power, DFT)

- Veloce Enhancements
  - Fast compile for gate netlist (Flat and hierarchical)
  - Small memory foot print for compilation
  - Ease of use like RTL flow
  - Functional verification no timing (SDF)

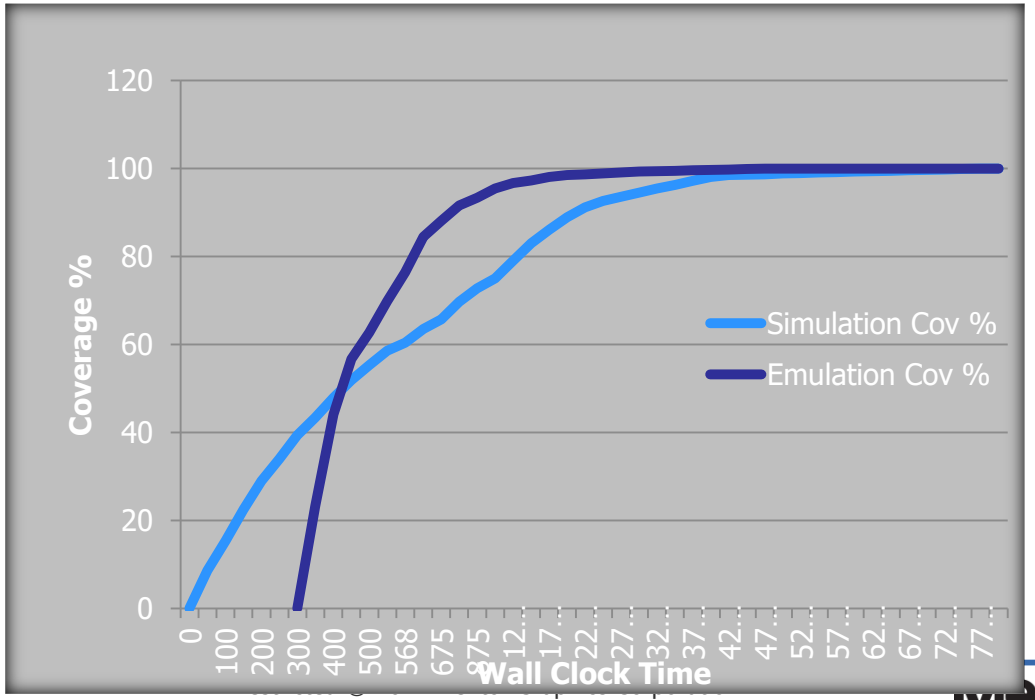
Veloce Coverage App: Assertion & Coverage



- Complete SVA assertion support
- SV Functional coverage: Covergroups, Coverpoints, bins, crosses and transition bins
- Code coverage: Statement, Branch, Toggle
- Standard UCDB support & merged with simulation UCDB
- Flow to enable XML merge with other platforms



ISO 26262



Mentor A Siemens Business

Complete Solutions by the Vertical Segments

5G | Networking | Storage | Multimedia | Mobile | Automotive | CPU | Mil Aero | ML/AI

Verification IP
Simulation Acceleration

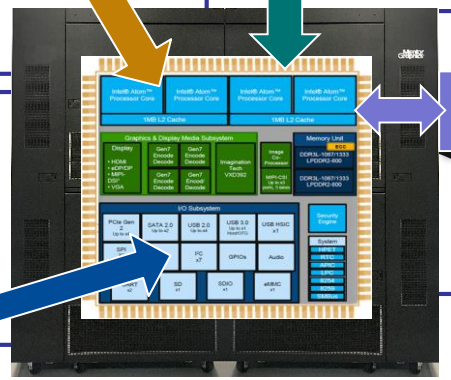
UVM · SYSTEMC · IEEE SystemVerilog

Memory
For ICE, Virtual ICE, Simulation Acceleration

VirtuaLAB

"Virtual" ICE
Enterprise-wide Virtual Platform
More Flexible than ICE

VTL



iSolve

ICE
iSolve speed adaptors

SoftModels

Mentor A Siemens Business

Accelerated VIP, Memory Models, Virtual Devices, and HW Peripherals (ICE)

Software-based			Hardware-based
SoftModel Memory Models	Accelerated VIP (Transactors)	VirtualLAB (Virtual ICE)	iSolve (ICE)
AMBA Slave (AXI, AHB)	AMBA (AXI-3/4, AHB, APB3/4, AXI4Stream) AHB 5 (**EA**)	Ethernet 1G/10G/25G/40G/50G/100G/200G/400G	Ethernet (small systems)
DDR2	AMBA (ACE, ACE-LITE)		Ethernet Switch (large port count)
DDR3 + DFI	AMBA 5 CHI	Multimedia: HDMI, DisplayPort, S/PDIF, RGB, YUV, I2S, PCM, DVI, HDMI Audio, Raw Bayer MIPI CSI-2 (EA)	Multimedia: HDMI, DisplayPort, S/PDIF, RGB, YUV, I2S, PCM, DVI, HDMI Audio, Raw Bayer MIPI CSI-2 (EA)
DDR4 + DFI	HDMI (Transmitter only): 1.4, 2.0 + HDCP 2.2, 1.4		
GDDR6	eDP 1.3 + HDCP 2.2 : eDP 1.4 (**EA**)		
eMMC 5.1	Ethernet 1G/10G/25G/40G/50G/100G/200G/400G		
Hybrid Memory Cube (HMC)	I2C		
HBM + DFI	I2S	PCIe Gen4/Gen3/Gen2/Gen1 Host	PCIe Gen3/Gen2/Gen1
I2C EEPROM	MIPI CSI-2	USB 3.1/2.0	PCIe Gen4 (**EA**)
LPDDR	MIPI DSI	SATA 6/3/1.5 Gbps	SAS 3/6/12Gbps (22.5G **EA**)
LPDDR2	NVMe 1.2 (Host) (EA)	UFS 2.0 (Peripheral)	SATA 6/3/1.5 Gbps
LPDDR3 + DFI	PCIe Gen3/Gen2/Gen1	JTAG Probe	USB 3.1/2.0 (Host)
LPDDR4 + DFI	PCIe Gen4 (**EA**)	NVMe Gen4/Gen3 Peripheral (**EA**)	UART
LPDDR5 (**EA**)	UART		JTAG Probe
ONFi 4.0 NAND Flash/Toggle DDR2 +DFI	USB 3.0/2.0/1.1 (Host)		
Samsung NOR Flash	SAS 3/6/12/22.5GBps		
SD Memory Card	SPI		
Spansion NOR Flash	V-by-One		
Strata Flash	CAN, CAN FD		
QSPI and Octa-Flash	LIN		
SPI NOR Flash	FlexRay (**EA**)		
	Automotive Ethernet (**EA**)		

Veloce Delivers Complete Verification Eco-System for Networking Designs

Networking

- Highest Comodeling Bandwidth
- Largest Capacity
- Native TCAMs

Platform

EcoSystem

Ethernet IP Providers

CoMIRA SOLUTIONS · More than IP · eSilicon · Avago Technologies

Testers

ixia · SAROKAL TEST SYSTEMS · SPIRENT

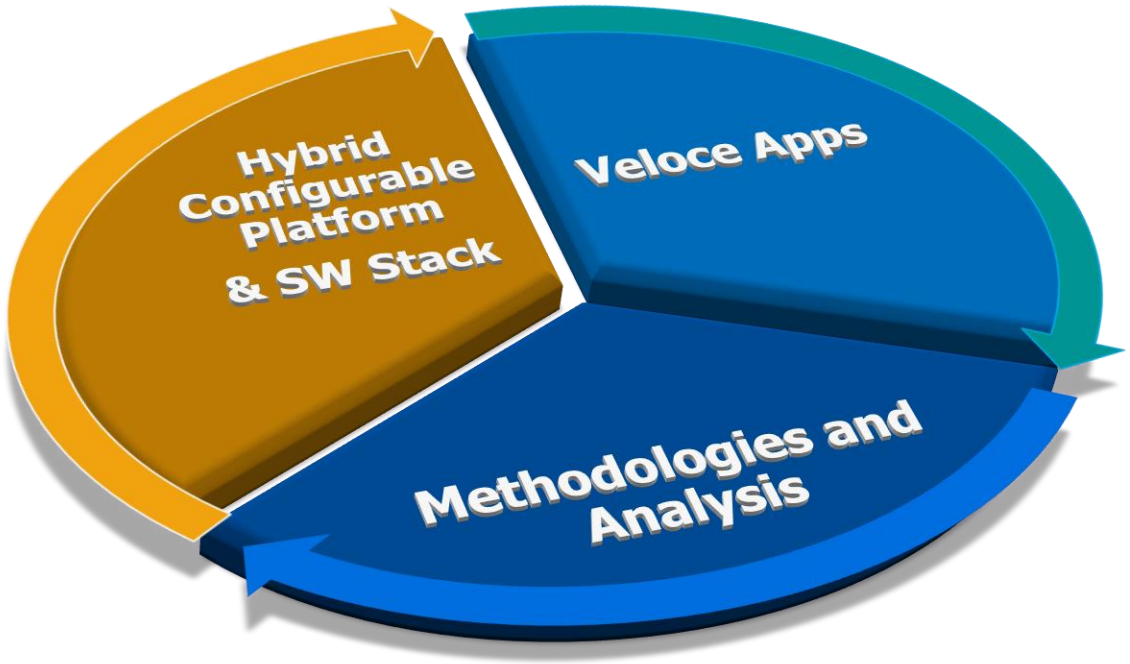
Apps & Solutions

- VirtuaLab Ethernet
- VirtuaLab PCIe
- ICE & Virtual ICE
- Deterministic ICE

Pre-silicon verification ← *Shift Left* → **Post-silicon lab test Software validation**

Mentor A Siemens Business

Veloce HYCON



- Is NOT just HYBRID!
  - Full featured platform
  - Includes a full SW stack
  - Fully integrated and compatible with Veloce Apps
- Opportunity to produce full-system power estimates and optimization pre-silicon in the context of real applications
- Example use cases:
  - SW Development; Power Analysis and SW Correlation; Performance Analysis; SOC Validation
- Allows for Multiple Usage Models
  - Pre-RTL; IP Integration; SoC Validation
- Provides a path from Pre-RTL (Early Architectural Analysis) -> IP Integration -> SoC Validation
- Delivers on the promise of "Shift Left"

Why Veloce HYCON?

Pre-RTL

IP Integration

SoC Validation

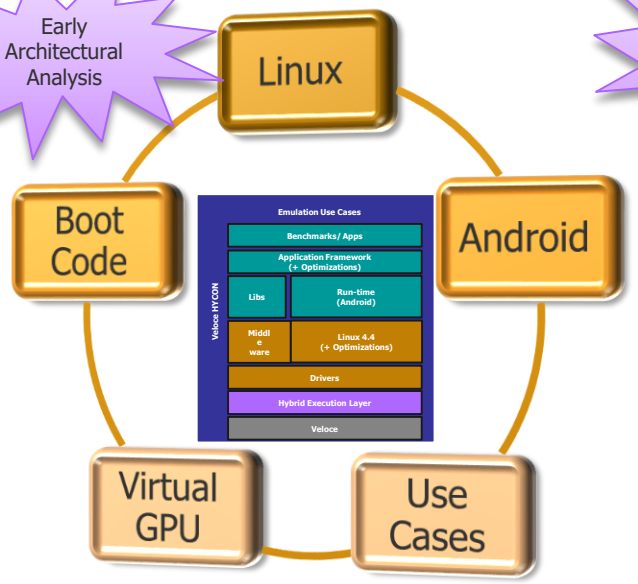
Early Architectural Analysis

SW Integration

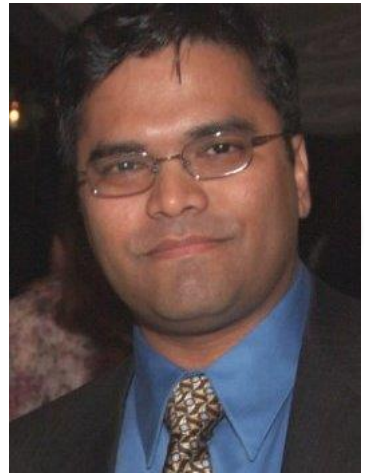
Performance Analysis

Power Use Case

SOC Validation



"With the Veloce Strato emulation platform we get more than just talk about 'shift left', we get technology that makes the shift left promise a reality in a way that can be easily executed in our existing verification environment." – Nasr Ullah Samsung SARC



HW Integration

RTL

3rd Party RTL

Hardware Development

Tape-out

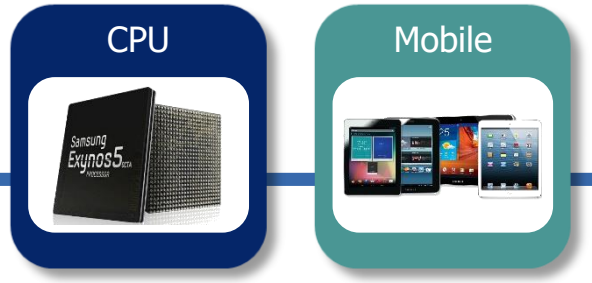
Typical SoC Validation

Run Applications/Benchmarks; Do workload analysis

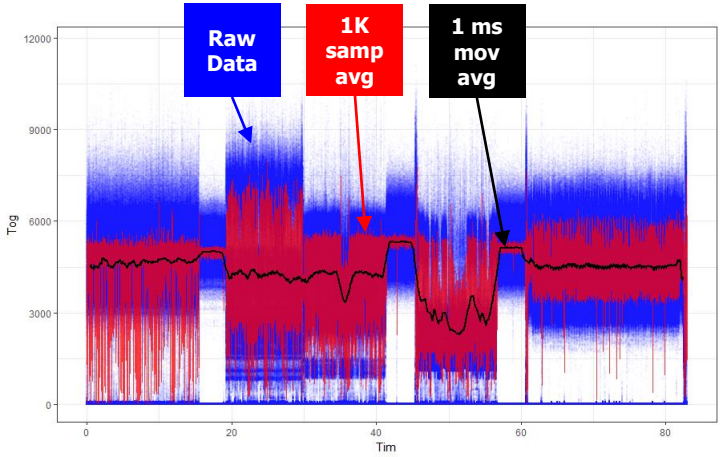
Early Power, Performance, SW & HW Integration

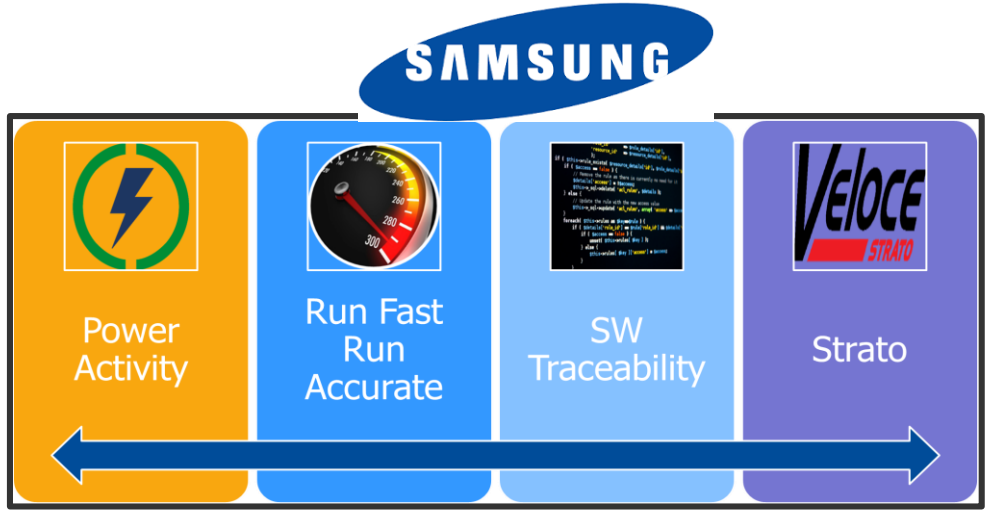
RTL Deploy (TO -1-2 Years) | TO – 9 months | TO – 2 months | Silicon Available

HYCON: SW-Power Correlation

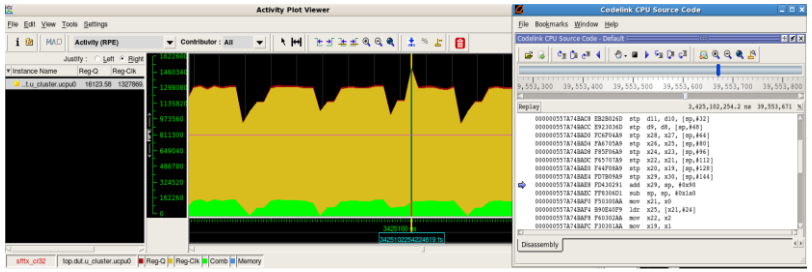


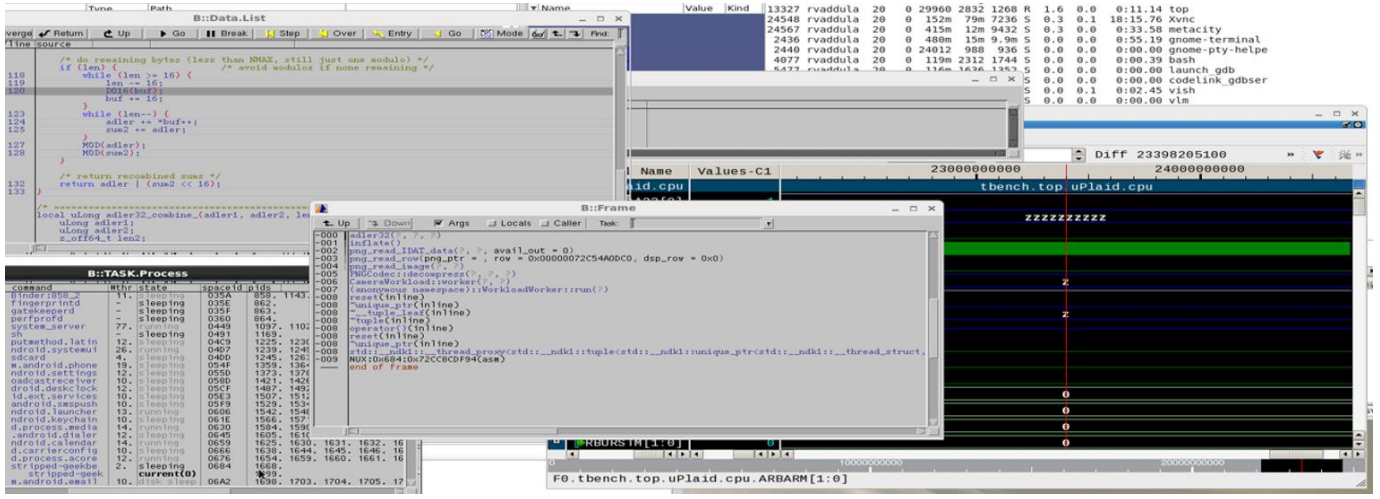
- Mobile CPU/GPU





Metric On Strato	Measurement
Compile Freq	1 Mhz
Time to Linux Boot	30 secs
RF to RA Switching time	<10sec

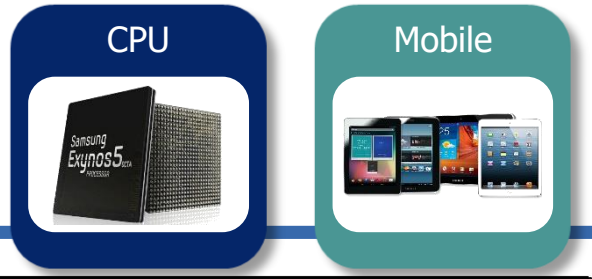


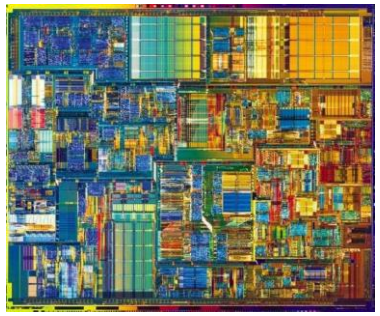


CPU Core running Geekbench

- Codelink
- Power peaks synchronization with SW instructions running on CPU

Veloce HYCON with Veloce Power App



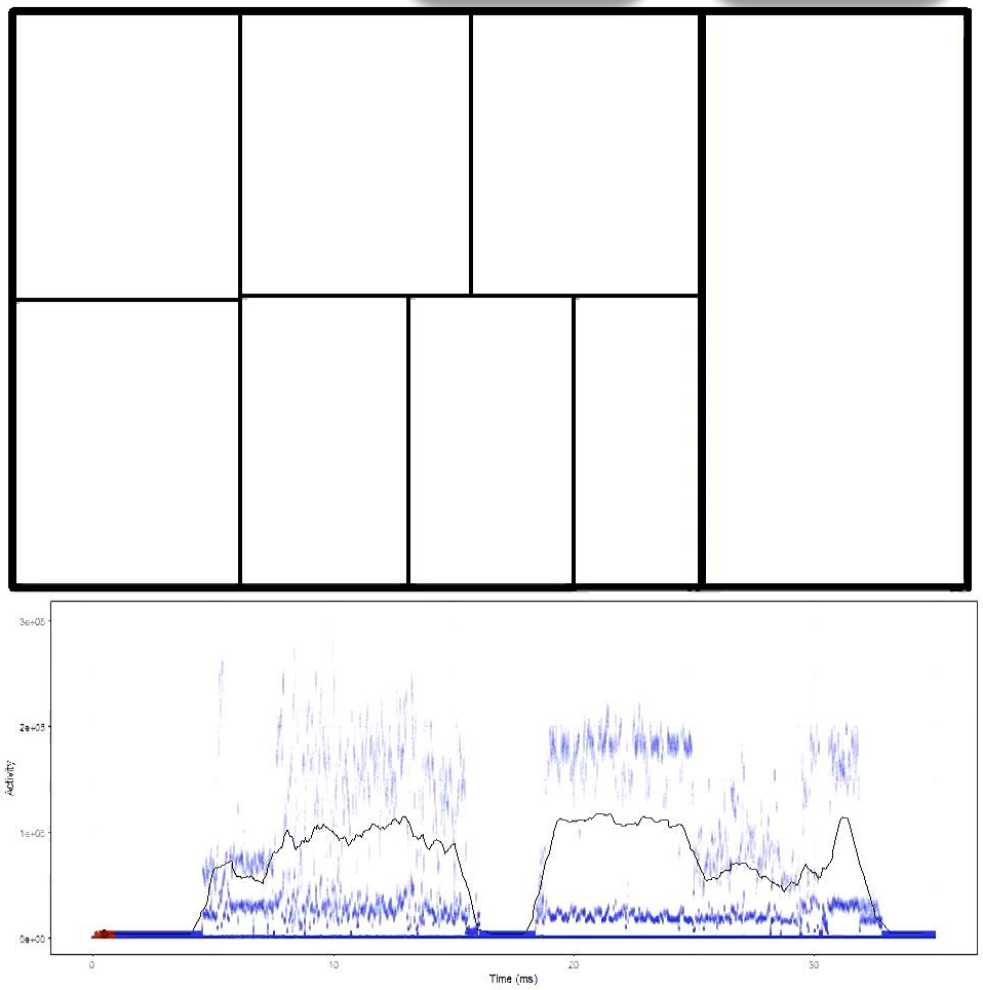


Handle Large SoC
(RTL/Gate)

Performance for Complete Verification (e.g. OS Boot) [100s Millions of Cycles !]

SPEED

Accurate Power Numbers Based on **Real Switching Activity**



Mentor A Siemens Business

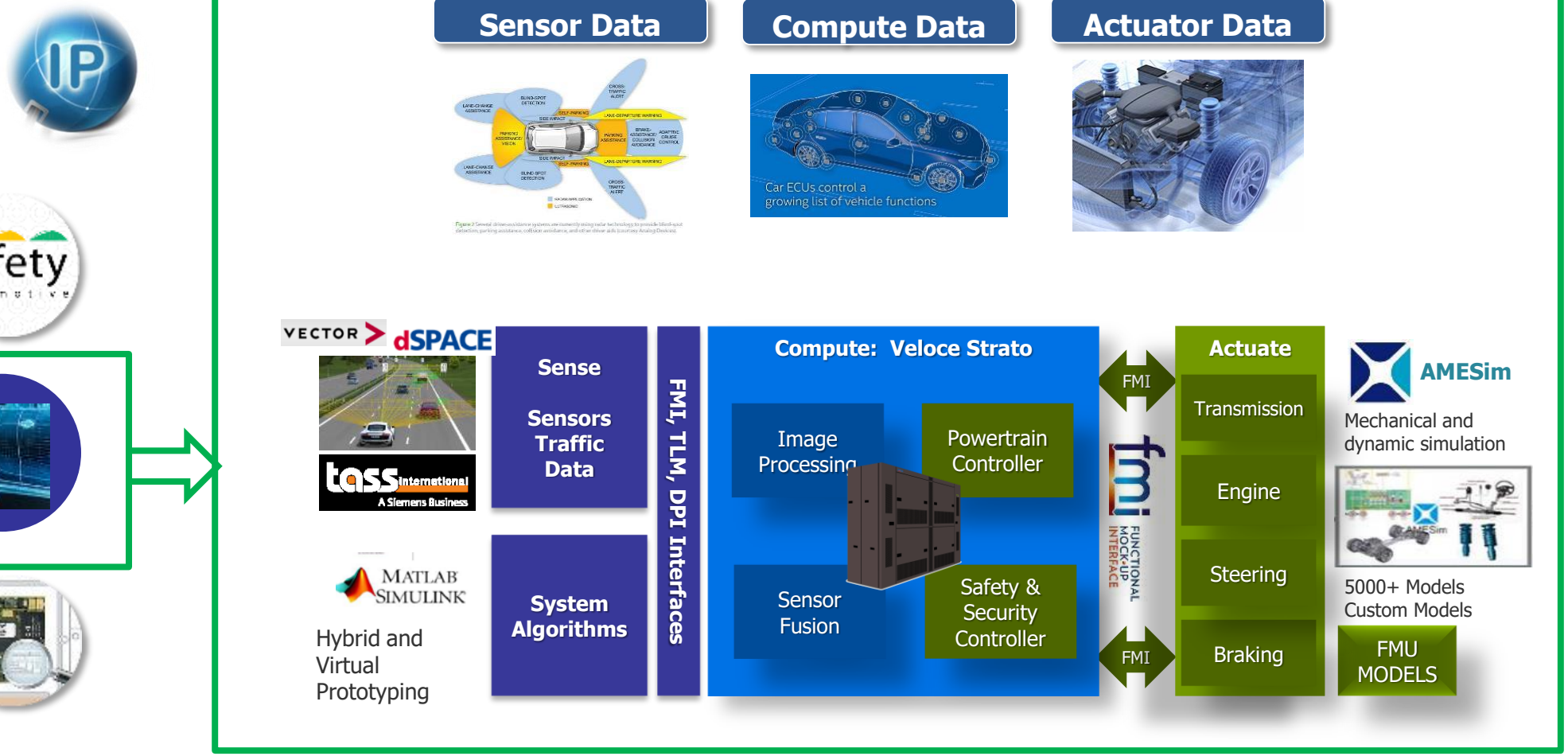
Automotive Strategy: Four Pillars

Veloce VIP
VTL transactors

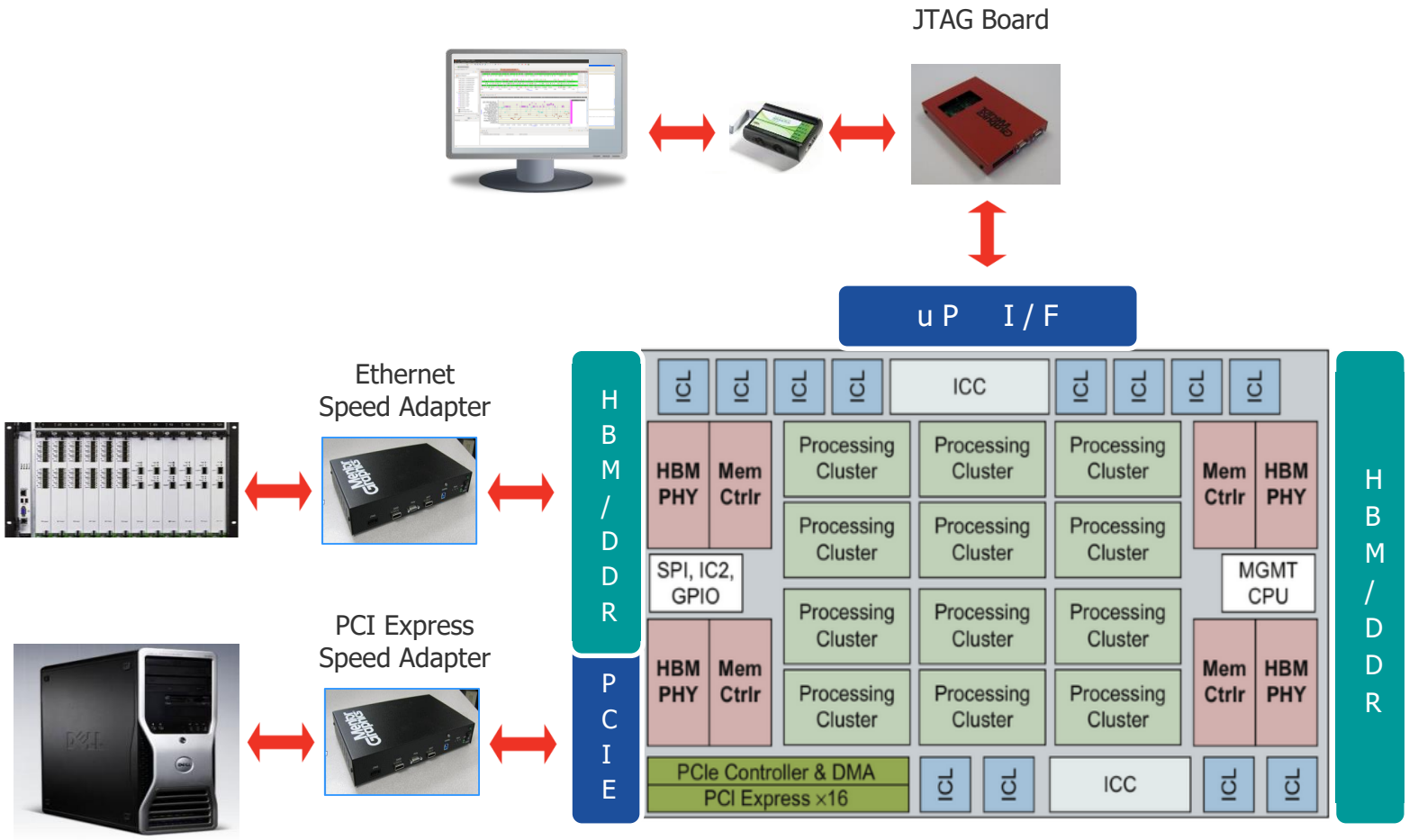
Functional
Safety

Automotive
Digital Twin

Security

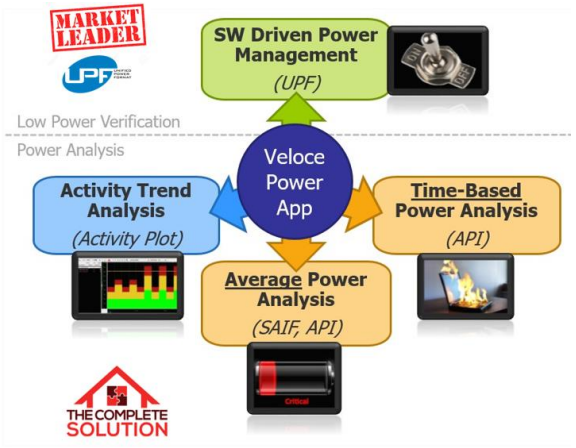


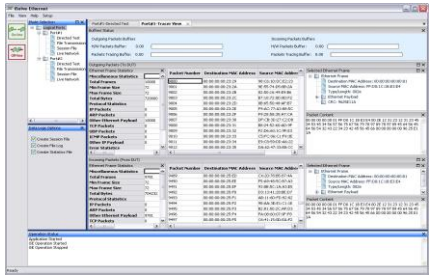
Machine Learning: ICE Solution



- Plug n Play
  - Real World Stimulus
- 1+MHz Perf
- Non-deterministic
  - De-ICE available
- Std Interface - speed gaskets available
- Perf Analysis

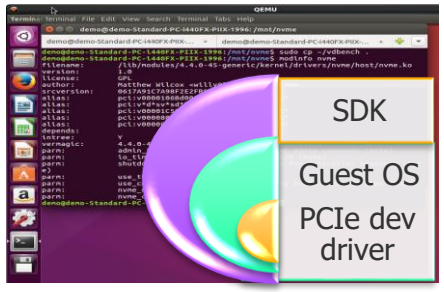
Machine Learning: Virtual Solution





Standard / Proprietary

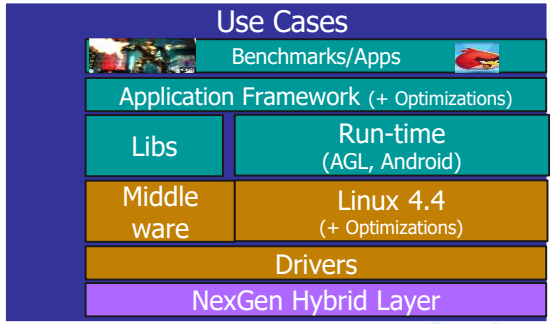
Ethernet



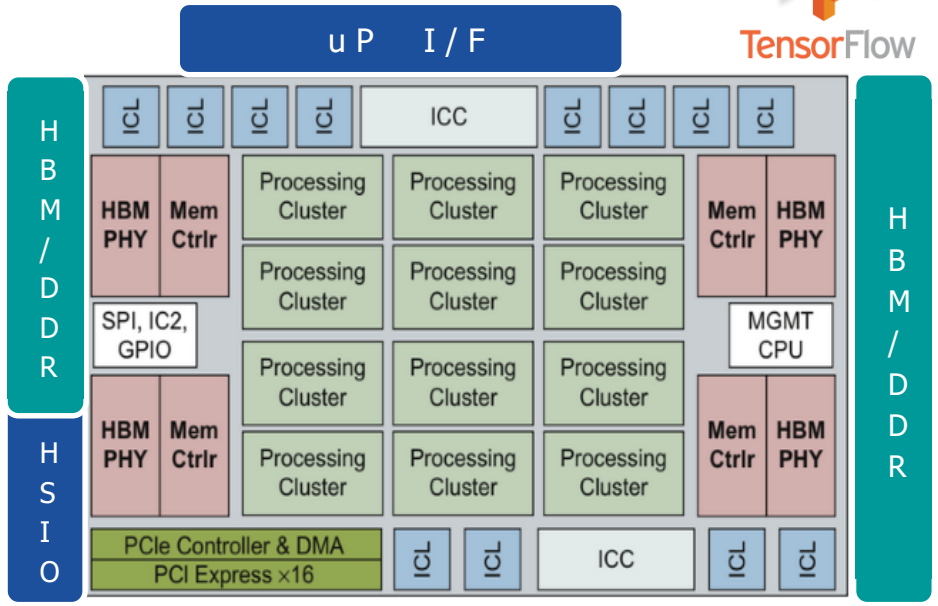
Standard / Proprietary

High Speed Protocol

Virtual JTAG



TensorFlow



- Plug n Play
  - Real World Stimulus
- 1+MHz Perf
  - SW Dev @ 50 Mhz
- Deterministic
- Standard/Proprietary protocol solutions
- Accurate Perf Analysis
- Deep Power Analysis

VELOCE STRATO OS

Veloce - Unique Roadmap of Innovation

Leading HW Foundation

- Capacity to emulate the largest systems
- Uncompromised visibility and debug
- Fast and predictable compile and bring-up
- Max throughput, near 100% utilization
- Lowest Cost of Ownership

Unique Operating System

- Multi users
- Multi-projects
- Multi-generation HW support
- Modular resources

Fault Injection | Virtual Network | Deterministic ICE | DFT | Enterprise Server | Hybrid

Power | Coverage/ Assertions | SW Debug | Protocol Solutions (VirtuaLAB, iSolve, Soft Models) | Visualization

HOT 100 EDN 2015

ISO 26262
Mentor Safe Certification

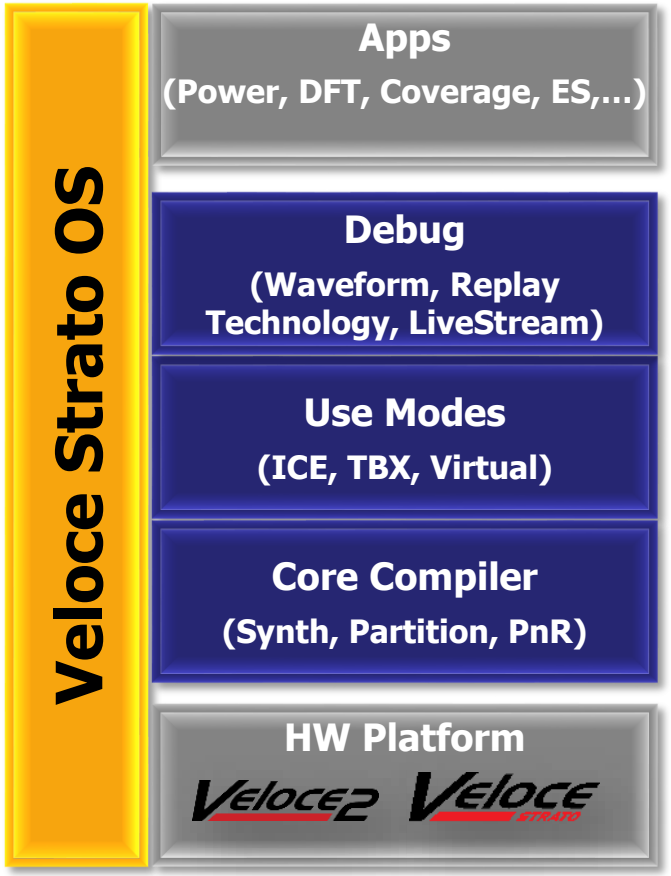
Segment Solution Leadership

5G | Automotive | IoT | Storage | Processor | Mobile/ Multimedia | Networking | Mil/Aero

Differentiating Applications

- Multi-verification applications
- Maximize capital ROI
- Optimize HW utilization

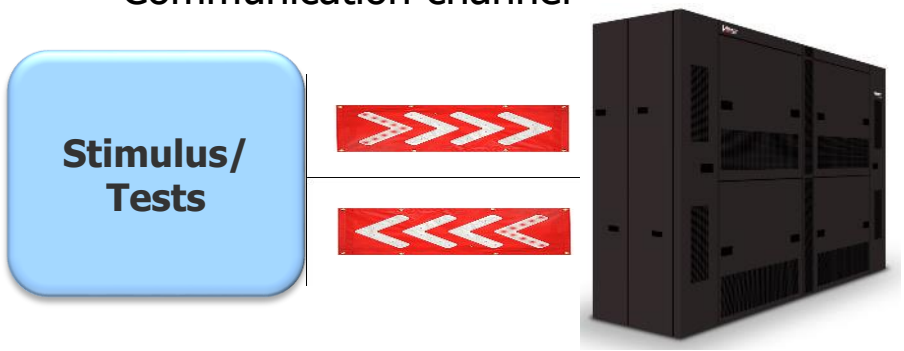
Veloce Strato OS - Verification Productivity



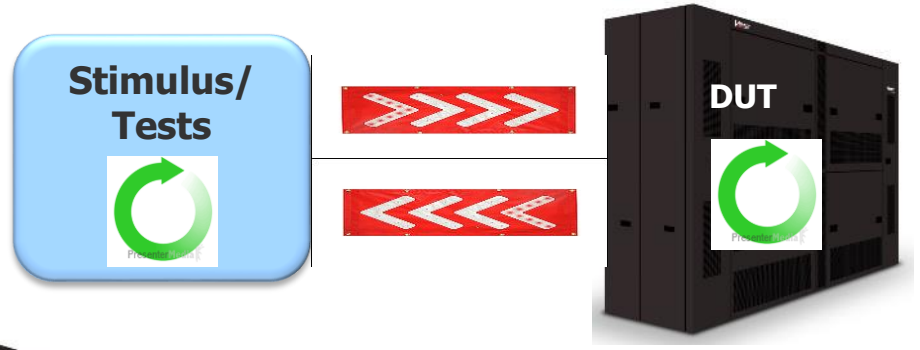
- Faster Compile
- SV Acceleration…
- Higher Throughput
- Faster Time to Visibility
- Incremental Force
- Flexible RTL Trigger
- Enhanced TCAM Modeling
- IP Protection
- Veloce Prototype Support
- ISO 26262 Certification

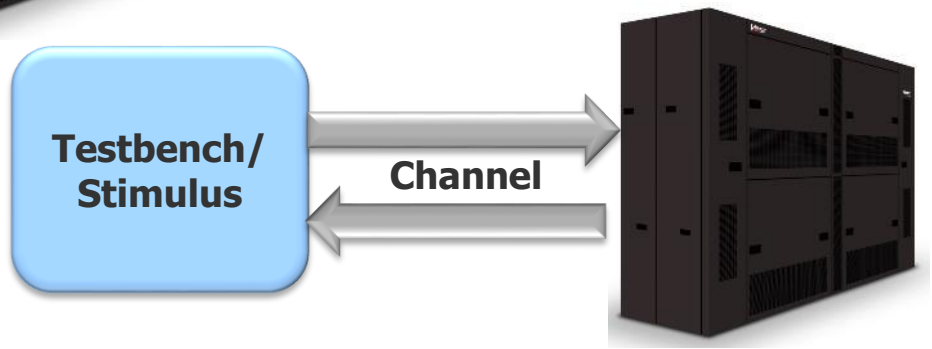
Fastest Simulation Acceleration

1 High bandwidth, low latency Communication channel

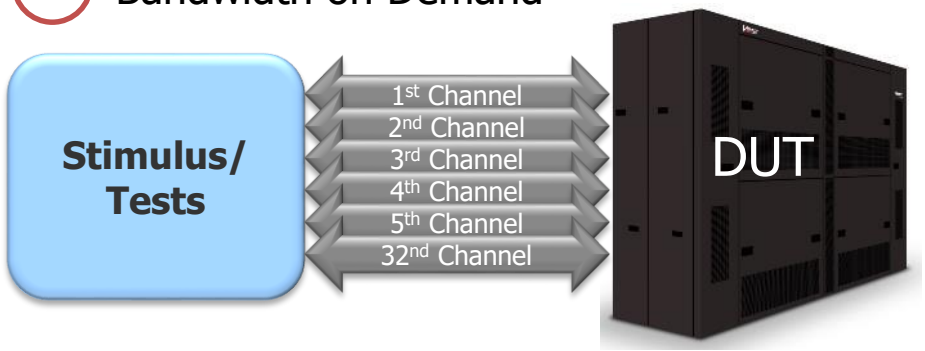


2 Parallel Execution (TBX) Deterministic Concurrency (Debug)





3 Bandwidth on Demand

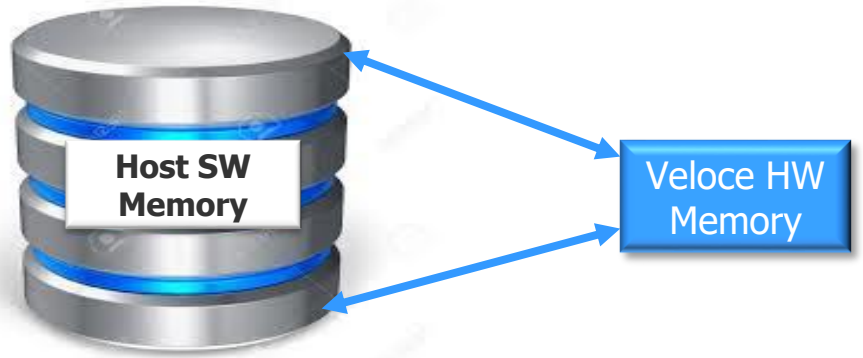


4 Fast and flexible Platform

Efficient Memory Map - Flexmem

- Veloce Flexmem - Overview
  - Automated construction of shared HW/SW system memory models
  - Large/multi ports memories
  - Optimal access from both SW and HW
    - Fast mem download/upload for large data images
- Advantages
  - Validate designs without modifying memories
  - Eliminates capacity impact from large system memories

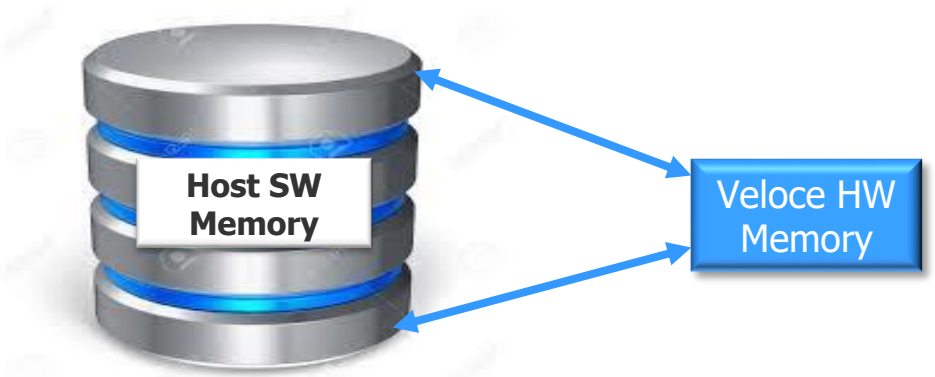
An efficient, flexible and easy way to map large memory map on Veloce



Veloce Flexmem

- Veloce Flexmem - Overview
  - Automated construction of shared HW/SW system memory models
  - Large/multi ports memories
  - Optimal access from both SW and HW
    - Fast mem download/upload for large data images
  - Minimal performance impact
    - Some scenarios it can improve performance

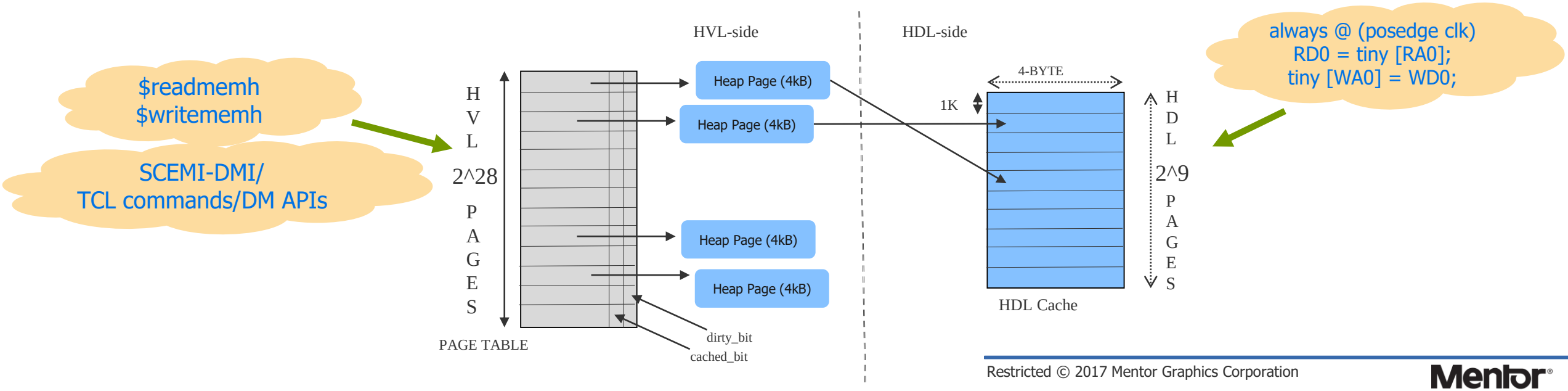
An efficient, flexible and easy way to map user defined memories on Veloce



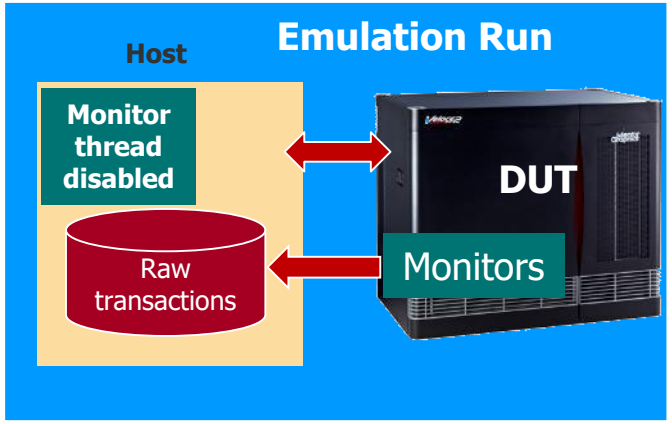
- Advantages
  - Validate designs without modifying memories
  - Eliminates capacity impact from large system memories

Veloce Flexmem – Details

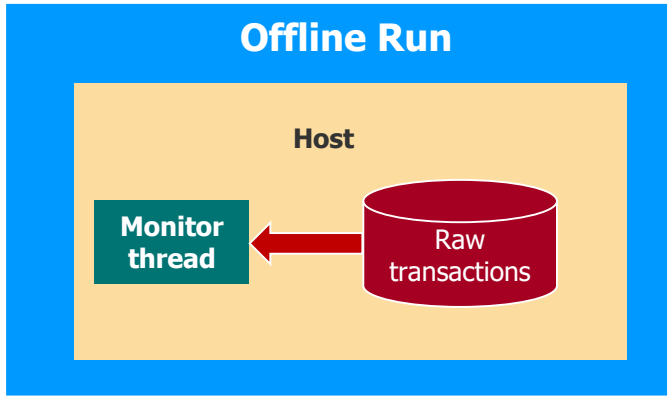
- Flexmem provides a view that user has 1TB on both HDL-side and HVL-side
- Allocates small percentage (< 1%) of RTL memory on the emulator
- The complete memory image resides on the HVL-side in the co-model process
- All the SCEMI-DMI/DM APIs/TCL/Verilog commands work on the HVL image
- DUT reads and writes work on the HDL cache image



Efficient Debug - Veloce Offline Monitor



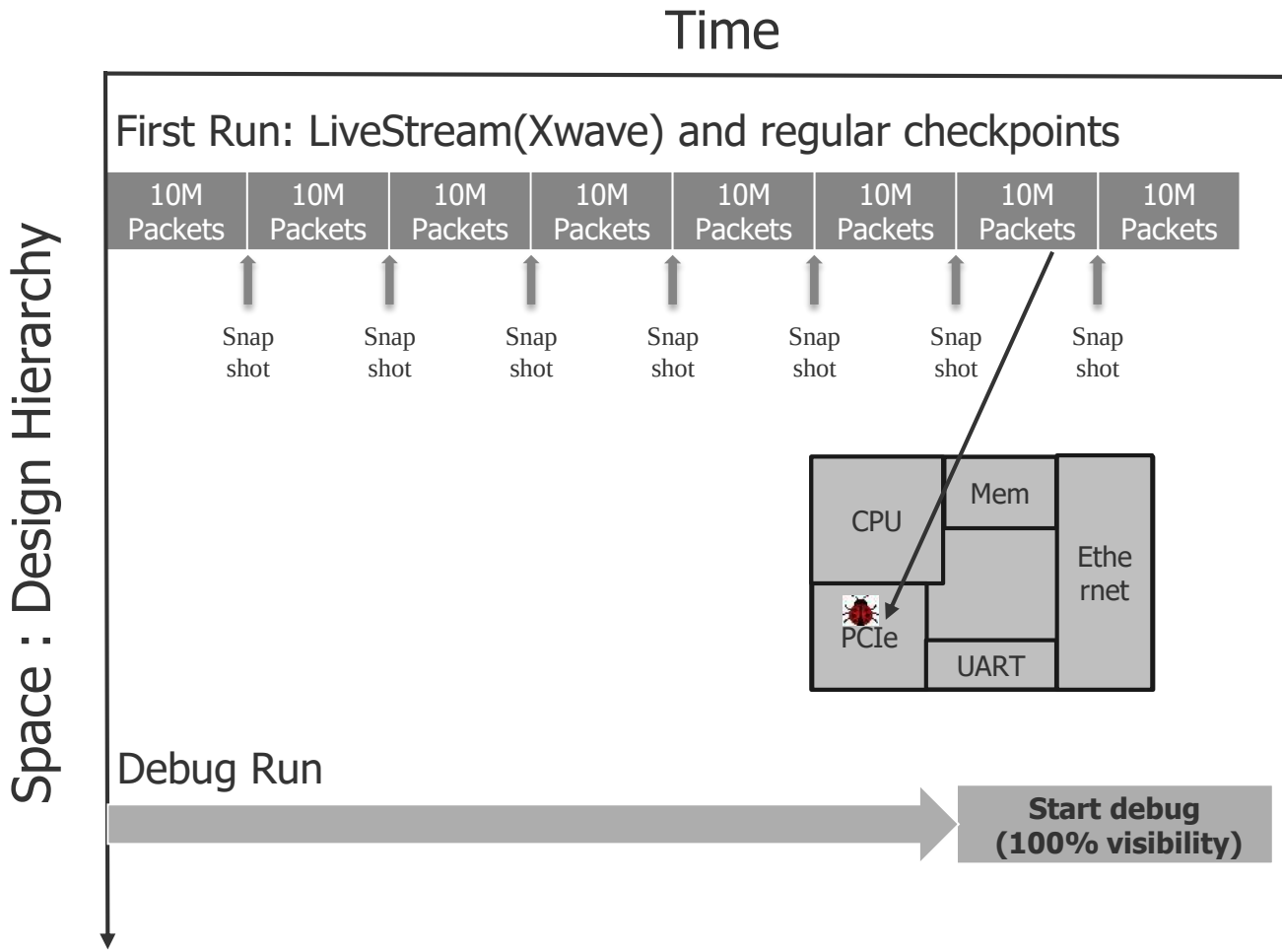
- Enable offline monitor flow at compile
- Run emulation with monitor process/thread disabled
- Veloce writes raw transactions to a file
- Example throughput improvement from 3% to 30% on a customer design



- Replay monitor process/thread offline with stored transactions
- Monitor processing overhead is eliminated from emulation run

Delivers increased emulator efficiency for monitor based debug (Decreased emulation time by 10X)

Efficient Debug – LiveStream & Checkpoint



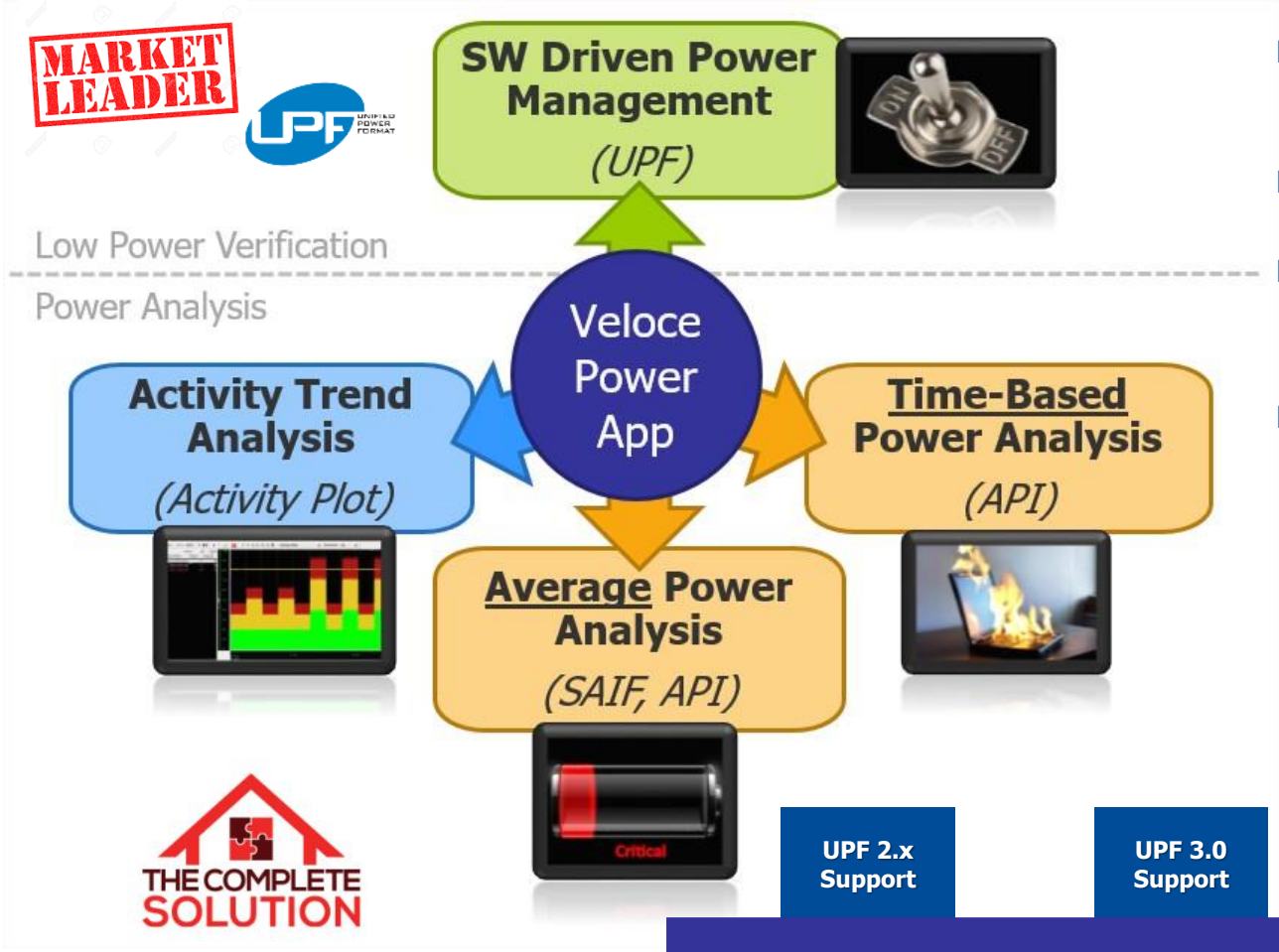
- First run
  - LiveStream: run emulation at full speed
  - Marching waveform (selected signals) for entire test duration
  - Chip performance analysis
  - Take regular checkpoints
- Debug run
  - Fast forward to the nearest checkpoint
  - Enable full debug: Assertions, Triggers, Waveforms, Monitors ….

VELOCE APPS

Veloce App Summary

- Overview of Veloce Application portfolio
  - Veloce Power App
  - Veloce Enterprise Server
  - Veloce Coverage App
  - Visualizer App
  - Hybrid App
  - DFT App
  - Fault Injection App
  - Deterministic ICE

Veloce Power App



- Low power verification at SoC level where power controls come from application SW
- Handle Large SoC (RTL/Gate) with Full Visibility
- Performance for Complete Verification (e.g. OS Boot) [100s of Millions of Cycles]
- Accurate Power Numbers based on real switching activity

Design	Size	#Cycle	File Flow	API Flow	X Factor
PCI Subsystem	42MG	11M	40 hours	5 hours	8x
Processor	65MG	15 M	51 hours	6 hours	8.5X
Video Enc-Dec	35MG	72 M	90 hours	8.5 hours	10.5x

Veloce + PowerPro Solution

NOW

Avg Pwr Est | Peak Pwr Est | Pwr Opt

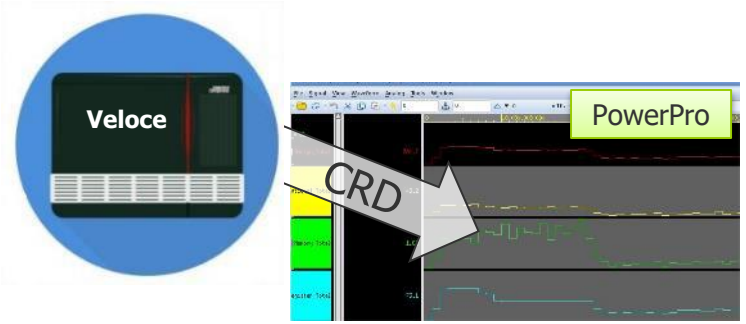
- **SAIF** support
- **SDPD SAIF** Support (State-Dependent, Path-Dependent)

Capacity support and complete Solution

2017 (Beta)

Avg Pwr Est | Peak Pwr Est | Pwr Opt

- **CRD** support
- Identification of time window of interest in Veloce -> analysis in PowerPro
- **Multi-CPU** space & time split

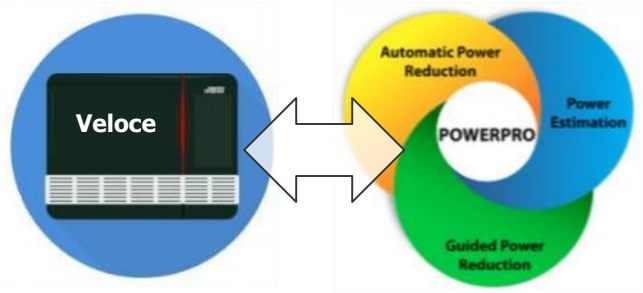


Leading Power Opt solution enabled

2017 (Beta)

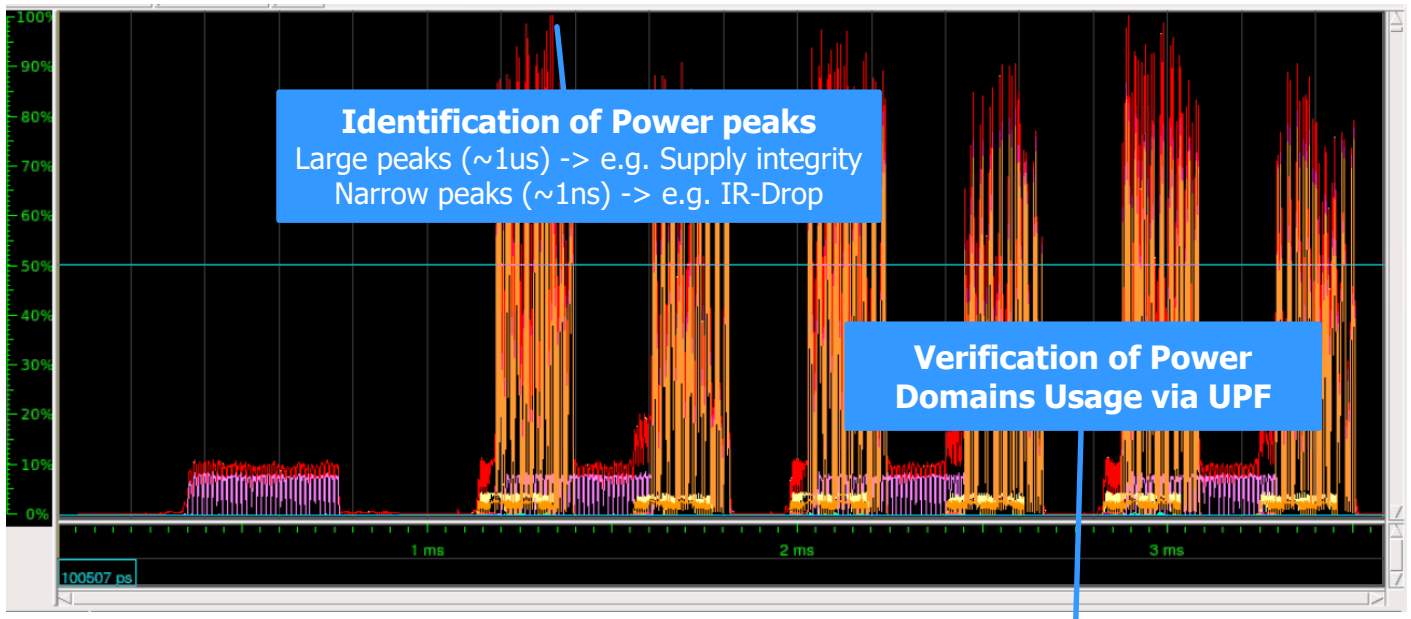
Avg Pwr Est | Peak Pwr Est | Pwr Opt

- **API** support
- No file handoff
- Live power plot
- 2-way data flow



Complete, Fast & Unique Power Flow

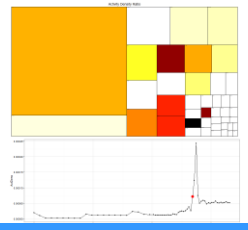
Power Analysis



Identification of Power peaks
Large peaks (~1us) -> e.g. Supply integrity
Narrow peaks (~1ns) -> e.g. IR-Drop

Verification of Power Domains Usage via UPF

Should be OFF

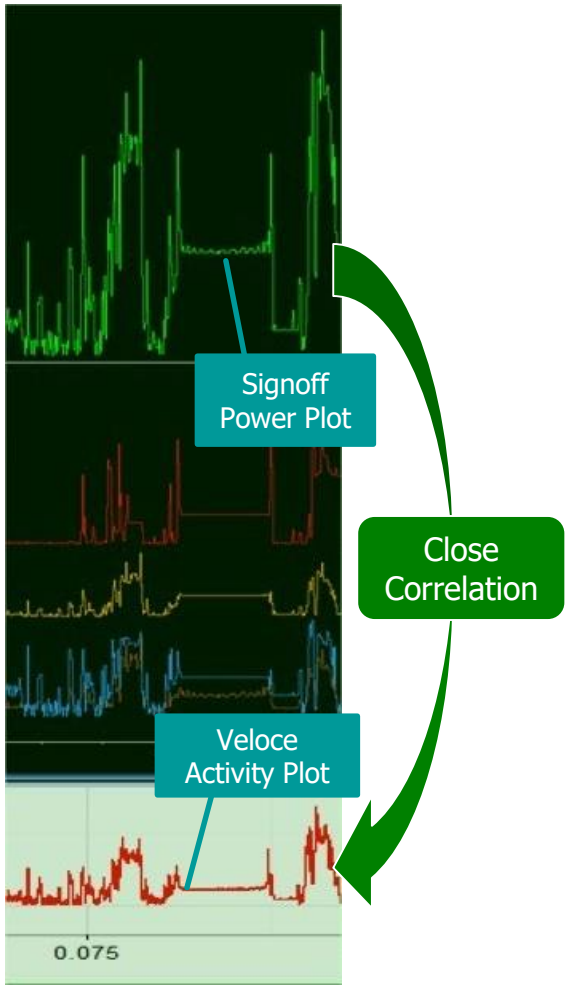


Hot Spots Identification
Optimization targets, Local IR-Drop,…

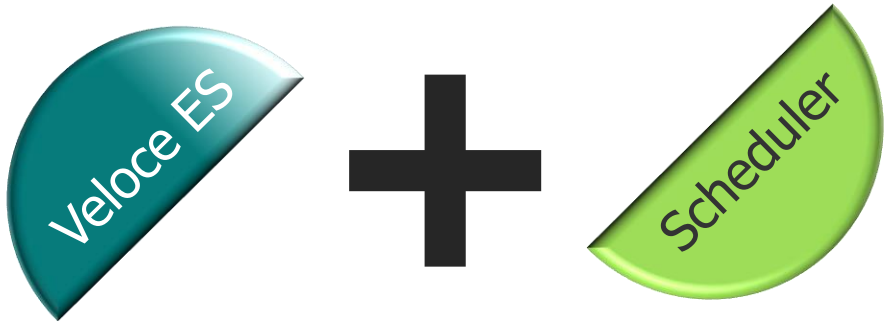
Power Surges Identification
dI/dt voltage drop

Electro-migration
High power on very long periods

Power Trends
Compare activity plots across RTL drops



Veloce Enterprise Server App



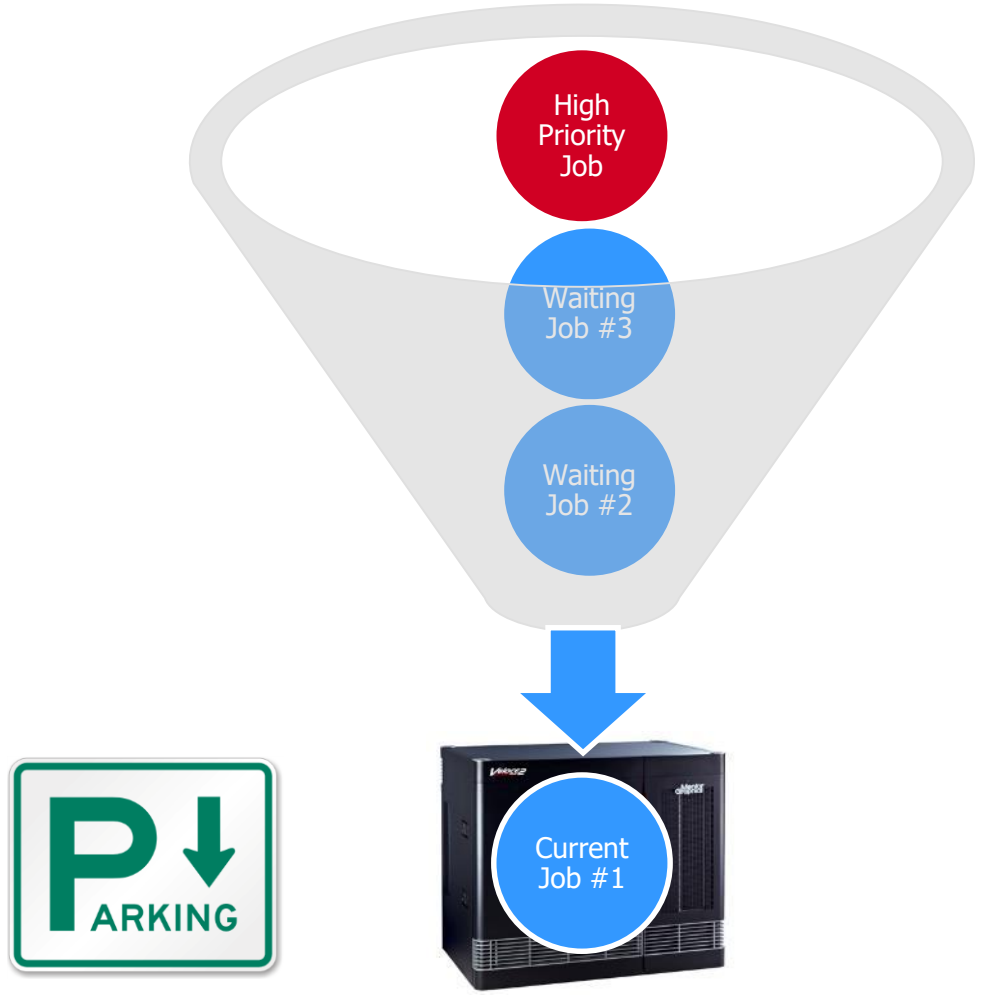
On Average 20%

Efficiency & Throughput gain

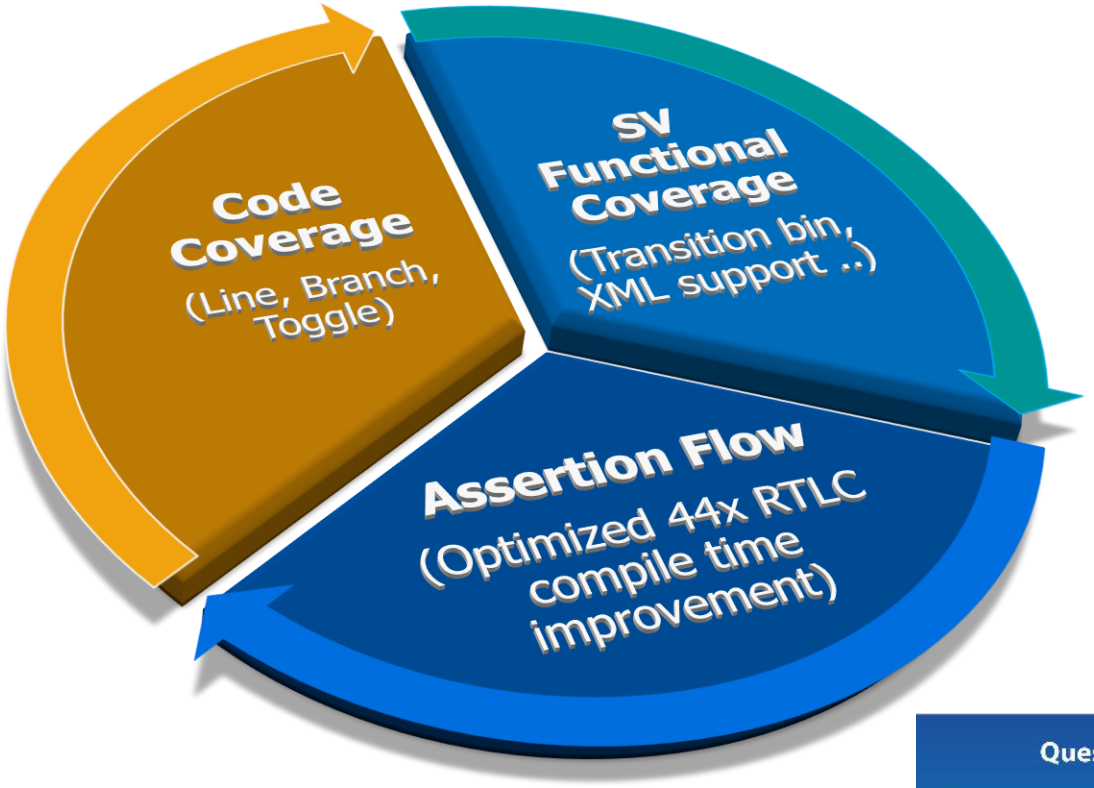
Features	Optimized HW allocation for a given job	LSF: Sold by Mentor IBM
	Service high priority jobs (Suspend/Resume/Relocate)	SGE: by Univa UNIVA
	View current Veloce status	NC: by RTDA Runtime Design Automation
	Generate Veloce HW Reports	APIs for custom scheduler
Benefits	Transparent access of Veloce HW by users	Rules-based solution for entire organization
	Maximize Veloce utilization	Flexibility to use preferred job management engine
	Track Veloce use by project	

Enterprise Server App

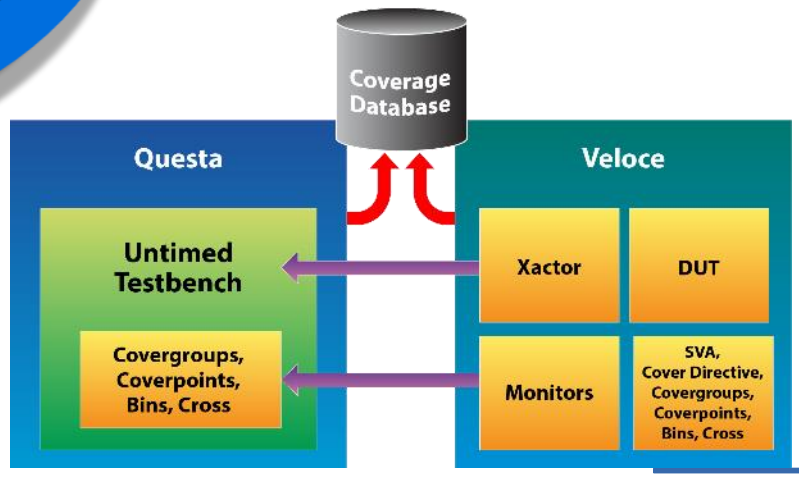
- Maximize Veloce utilization & sharing
- Automated job scheduling & prioritization
- Flexible Veloce sharing by multiple teams worldwide
- On-the-fly utilization reports
- Support LSF, SGE, NC or custom



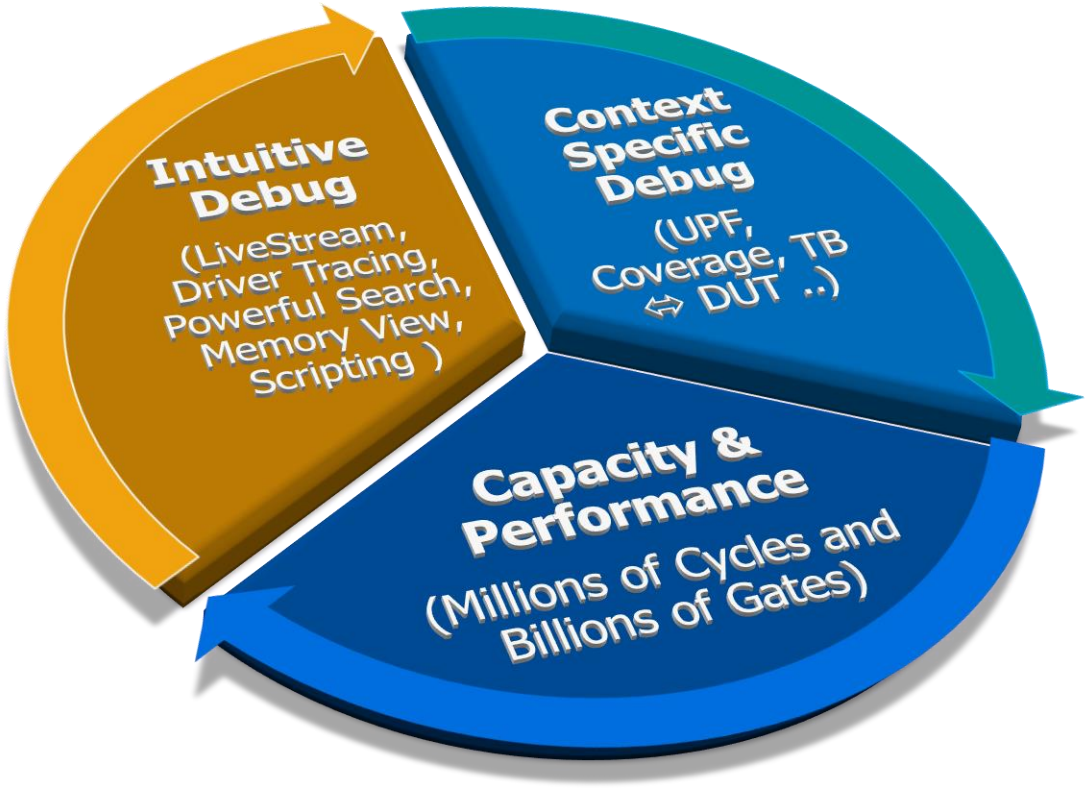
Veloce Coverage App



- Hard-to-reach corner cases requiring millions of clock cycles
- Coverage collection using real-world stimulus
- Boot OS and collect coverage while running software
- Coverage for safety compliance



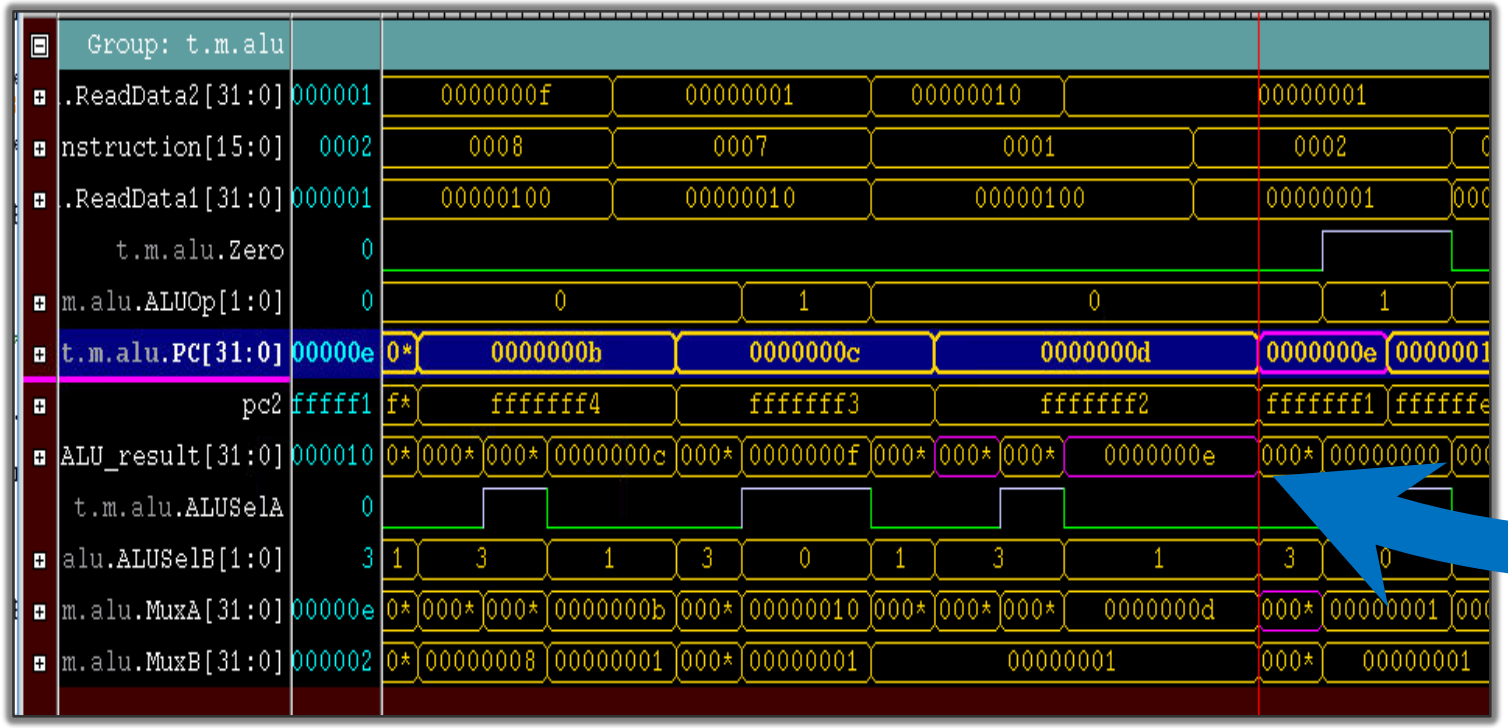
Visualizer App

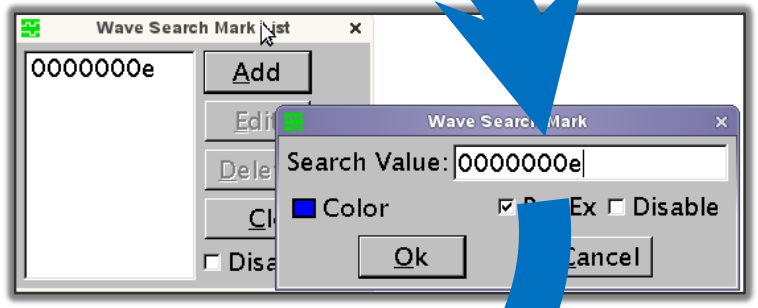


- Common platform for Veloce, Questa, Veloce Prototyping System
- Competitive debug environment compared to other debug tools
- Short learning curve for transition from other debug tools

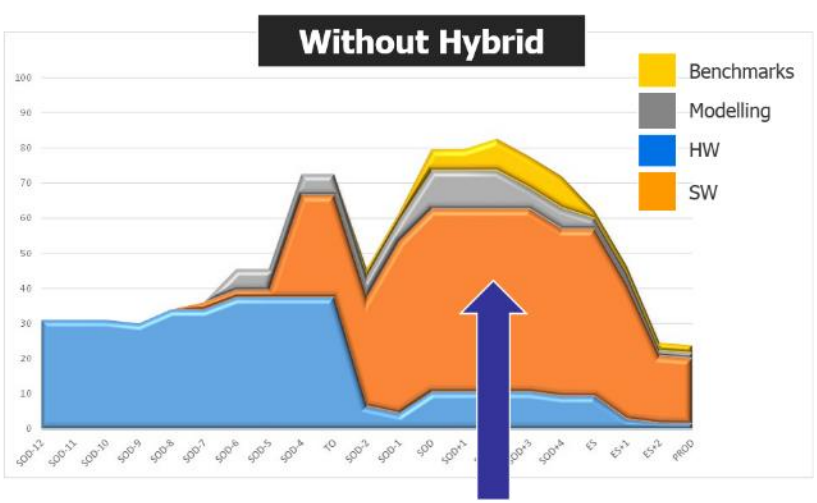
Visualizer - Powerful, Easy Searching and Filtering

- Search and Filter in any window to find objects
- Biometric search adds color tags to a search so that it is clearly highlighted in the waves

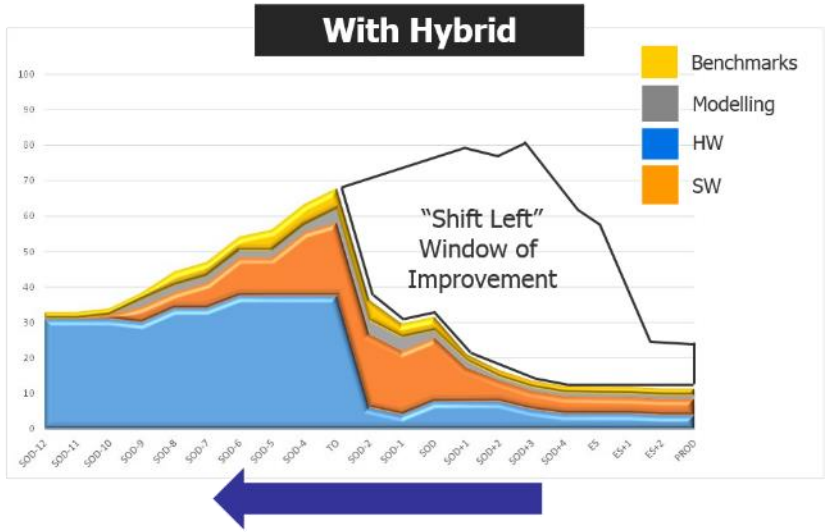




Veloce Hybrid Platform enabling early SW Development



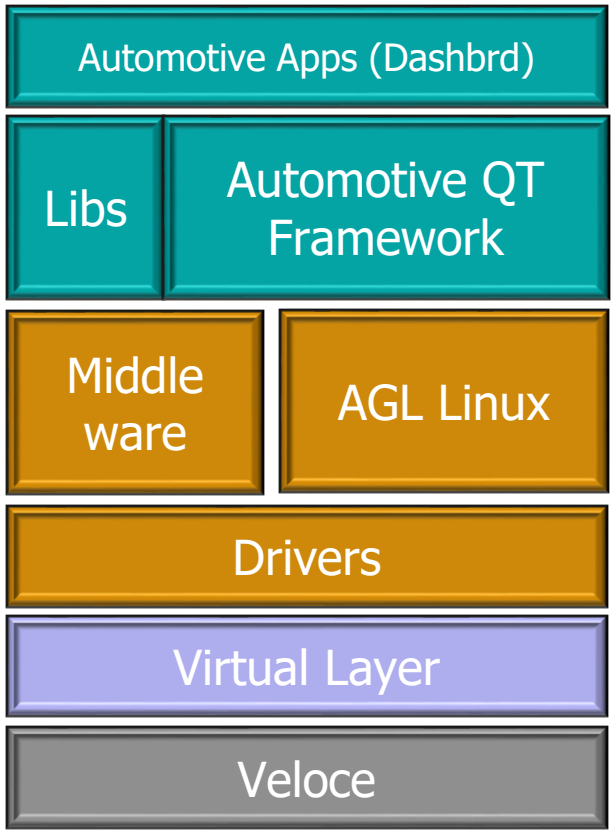
Limited early access to a stable HW platform in the SW phase, extends the SW development & validation effort



Early Hybrid SW platform, reducing SW cycle by weeks

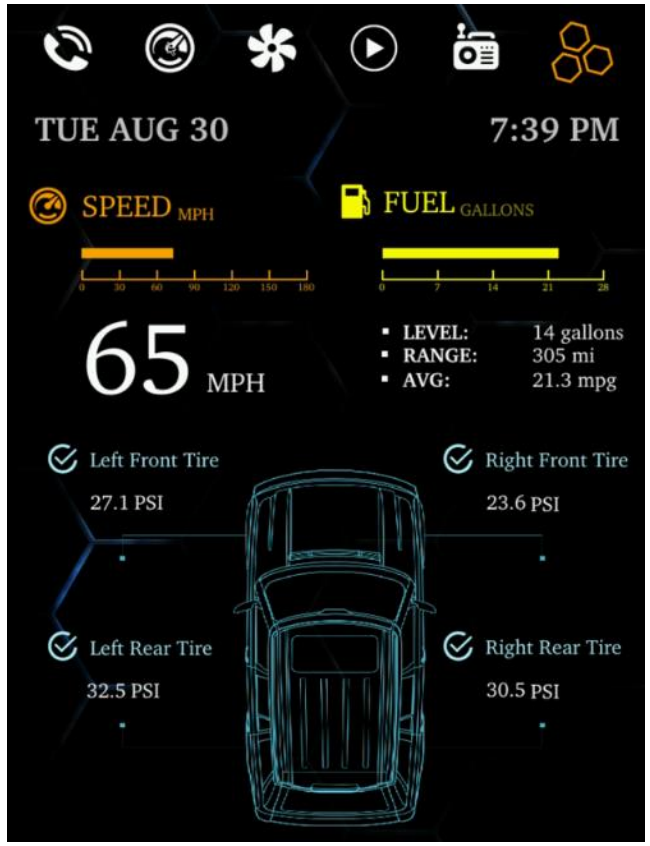
- Veloce Hybrid enables early access to a shared SW reference model for SW teams
- Model running at speeds of +30Mhz with OS boot in minutes
- Large development cycle reduction, enabling SW teams access to a development-debug platform long before early Silicon or FPGA prototypes are available

Hybrid- Automotive Grade Linux Demonstration Reference Platform For Automotive



Software Stack
On top of Virtual CPU & Veloce instrumented RTL

- Hybrid example running AGL Stack (Automotive Grade Linux)
  - AGL Linux drivers
  - AGL video using QT
  - AGL apps (HVAC, etc)
- The reference platform can execute the demo "out-of-the-box". Linked to customer RTL on Veloce
- Software execution speed of +30MHz
- OS time to Boot 3mins

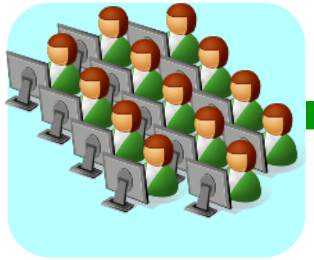


Screenshot of Hybrid Running *AGL Demo

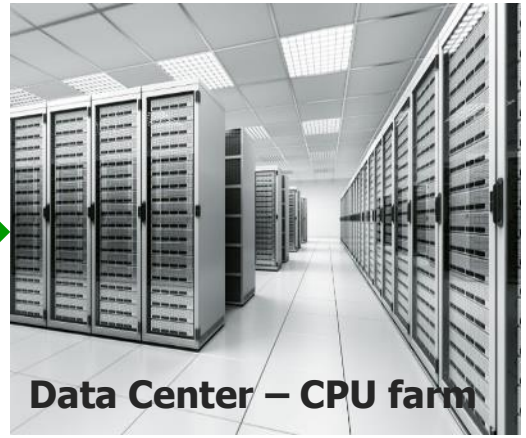
System Validation of Automotive Designs in the context of automotive software

Veloce DFT App : Accelerate DFT Verification

DFT Verification Unit Delay Patterns



DFT Verification Patterns with SDF

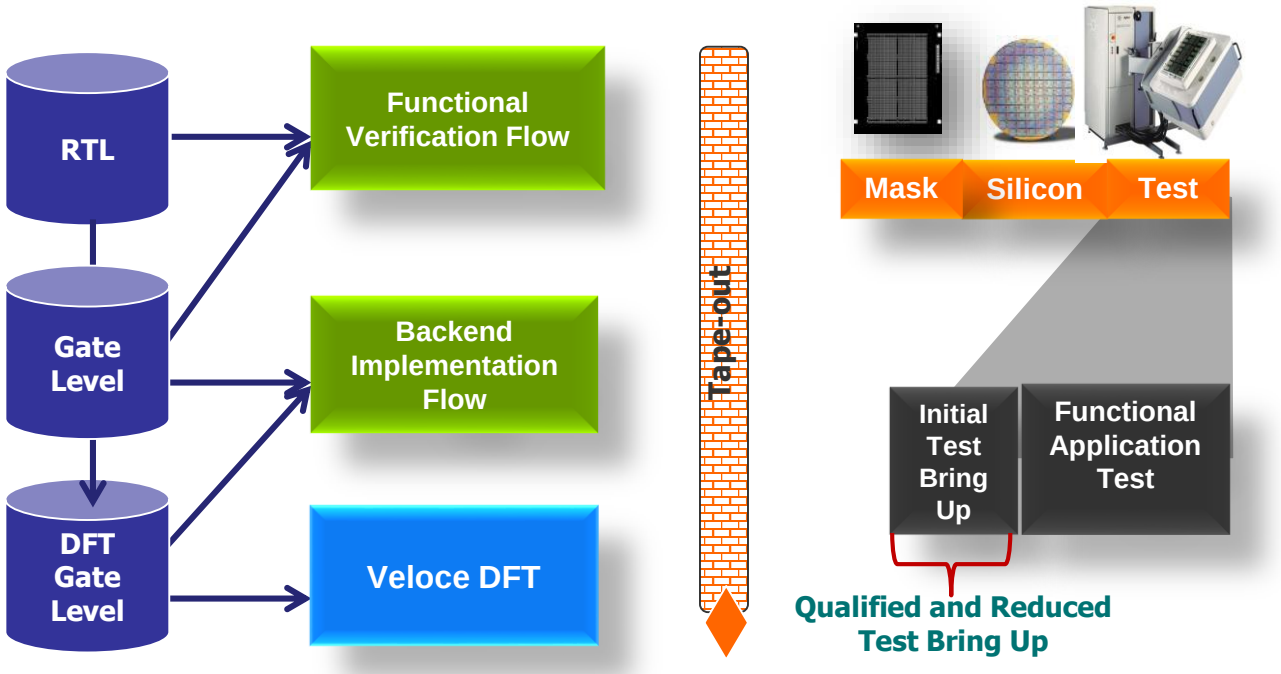


Accelerate unit delay patterns using Veloce

- Achieve faster overall DFT verification
- Ensure entire DFT verification flow is done before tapeout signoff

Simulate patterns with SDF back annotated using CPU farm

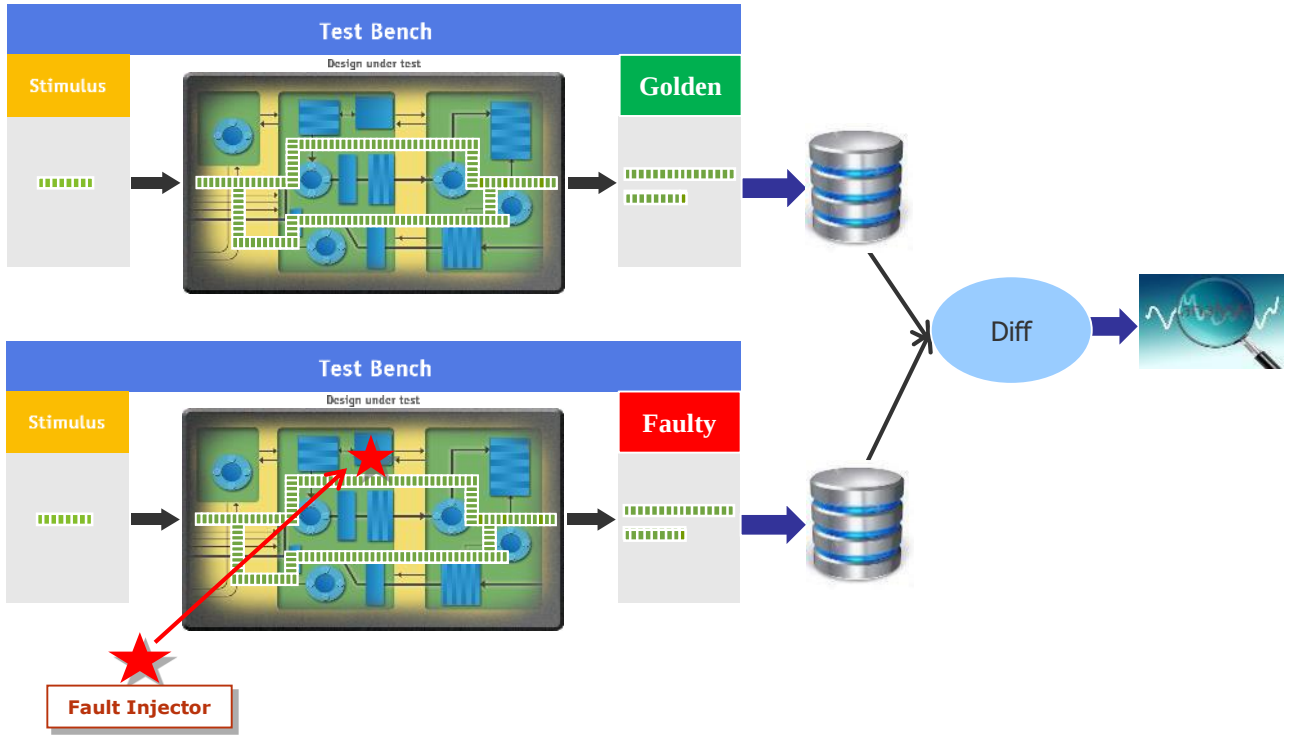
Veloce DFT App



Design	DFT Simulation	Veloce DFT	Improvements
Sensor	3.1 days	90 sec	3000x
WideIO	83.3 days	120 min	1000x
Graphics	2.7 days	58 sec	4000x

- Verification of DFT logic and BIST structure
- Increased pattern correctness, robustness, reliability
- Pre-tapeout pattern validation, acceleration of time to production
- Reduction of ATE test time and costs

Veloce Fault App

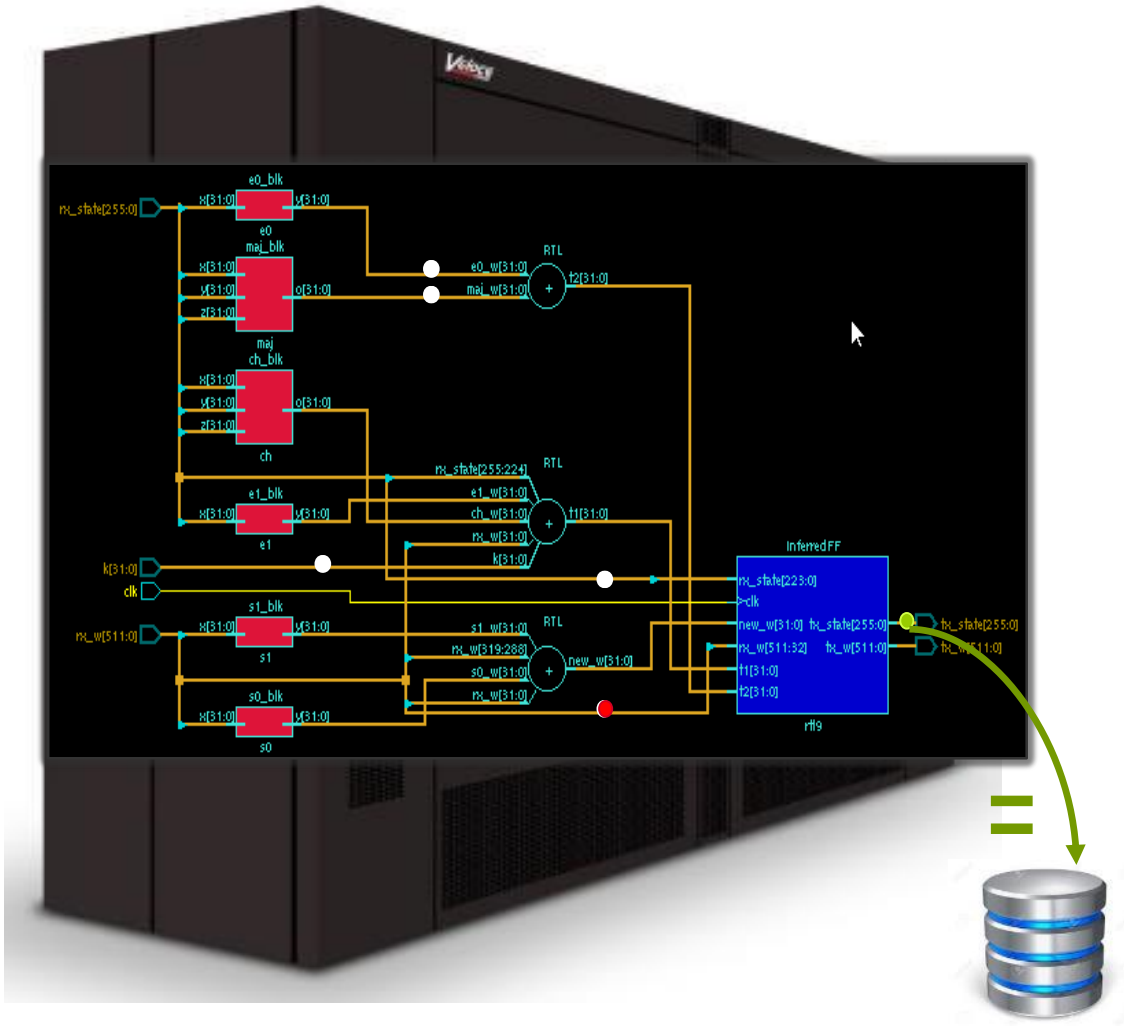


ISO 26262

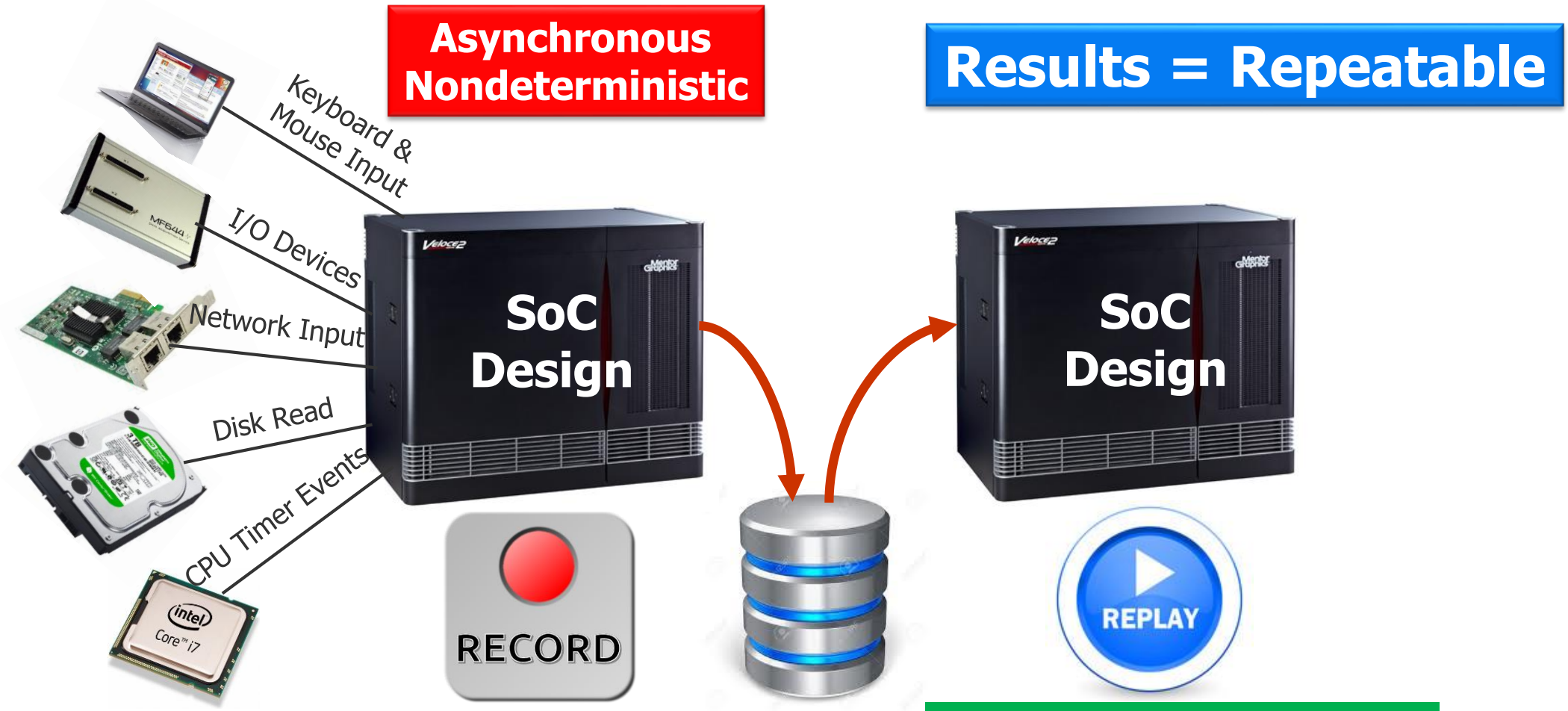
- Emulates design behavior in presence of structural faults
- Measures Fault Tolerance of design
  - Inject different types of structural faults
    - Types: Stuck at 0/1, Transition, Bridging fault
  - Monitors effects of faults
- Automates comparison of values from a golden run vs a faulty run
  - Reports mismatches at runtime
- Important for safety critical industries (automotive, aerospace, military)

Veloce Fault App

- Perform system level safety circuit verification
  - Ability to detect and respond to fault conditions
- Fault list compiled with design RTL or Gate Netlist
  - Fault site and type identification
  - Fault Detection Net(s) identification
- Golden Veloce run with no faults
  - Capture reference FDN behaviour
- Veloce run with fault enabled
  - Compare FDN behaviour against reference and report any mismatch



Deterministic ICE
Extending Virtual Advantages to ICE



VELOCE – INDUSTRY SEGMENT SOLUTIONS

Veloce - Unique Roadmap of Innovation

Leading HW Foundation

- Capacity to emulate the largest systems
- Uncompromised visibility and debug
- Fast and predictable compile and bring-up
- Max throughput, near 100% utilization
- Lowest Cost of Ownership

Unique Operating System

- Multi users
- Multi-projects
- Multi-generation HW support
- Modular resources

Fault Injection | Virtual Network | Deterministic ICE | DFT | Enterprise Server | Hybrid

Power | Coverage/ Assertions | SW Debug | Protocol Solutions (VirtuaLAB, iSolve, Soft Models) | Visualization

HOT 100 EDN 2015

ISO 26262
Mentor Safe Certification

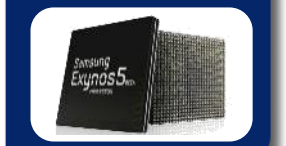
Segment Solution Leadership

5G | Automotive | IoT | Storage | Processor | Mobile/ Multimedia | Networking | Mil/Aero

Differentiating Applications

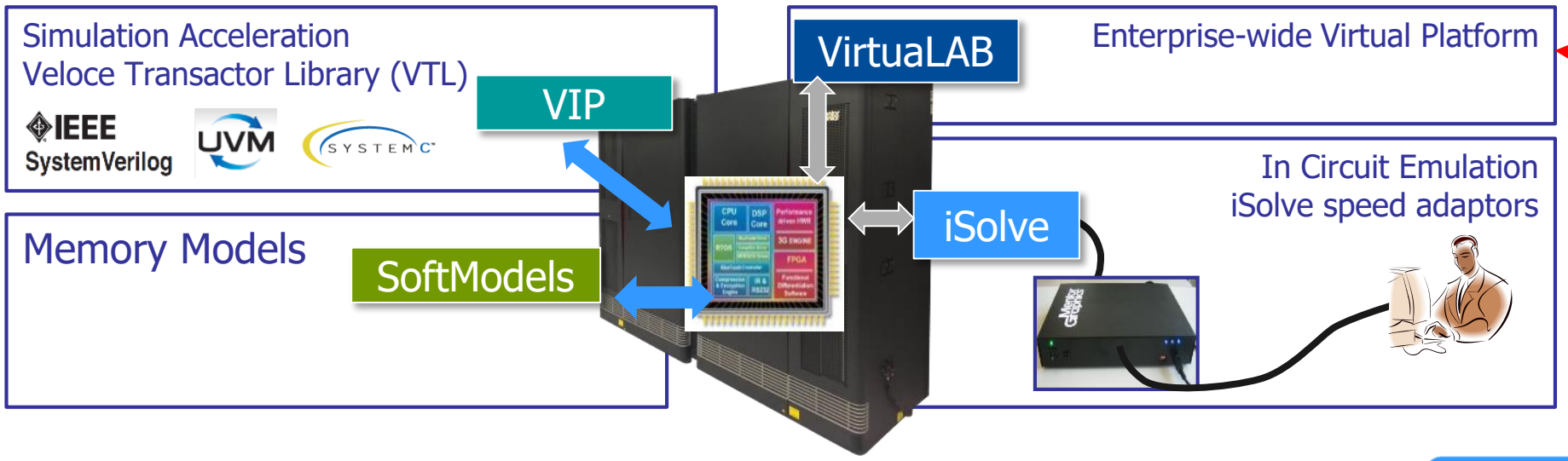
- Multi-verification applications
- Maximize capital ROI
- Optimize HW utilization

Vertical Market Solutions and Horizontal Apps

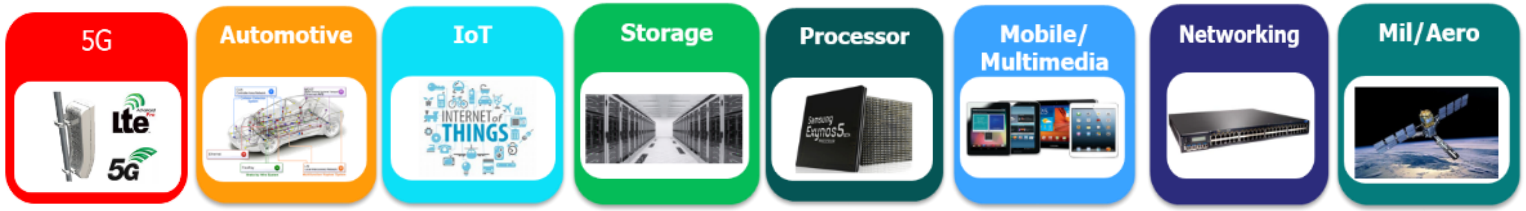
IoT	Networking	Storage	Mobile	Multimedia	CPU	Automotive	Mil Aero	5G
								
PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	Ethernet	PCIe	CPRI
Ethernet	Ethernet	Ethernet	AMBA	AMBA	AMBA	CAN	Ethernet	eCPRI
RGB	DDR	AMBA	MIPI	HDMI	DDR	LIN	DDR	OBSI
ONFi		SAS/SATA	UFS	DP/eDP		FlexRay		JESD
SATA		NVMe	DP/eDP	DDR		DDR		SPI
USB		UFS	DDR					
MIPI		ONFi						
UFS		DDR						

Security Fault — **System Performance Power** — **Coverage Assertions** — **DFT Software Development** — **Hybrid D-ICE**

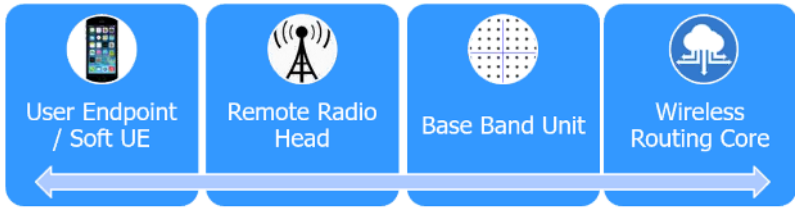
Driving Complete Solutions for Vertical Market Segments



CPRI
eCPRI
OBSAI
JESD
SPI



Unique SW solutions tailored for each Segment



Veloce enabled 5G End to End Platform

VELOCE
CUSTOMER TESTIMONIALS

Veloce continues to lead across multiple Markets

Installed base: 4000+ Veloce2 AVB2 installed WW with more than 90 different customers – over 70 Billion emulation gates installed *

8 of the 10 top telecom/networking companies have shifted to use Veloce during past 3 years

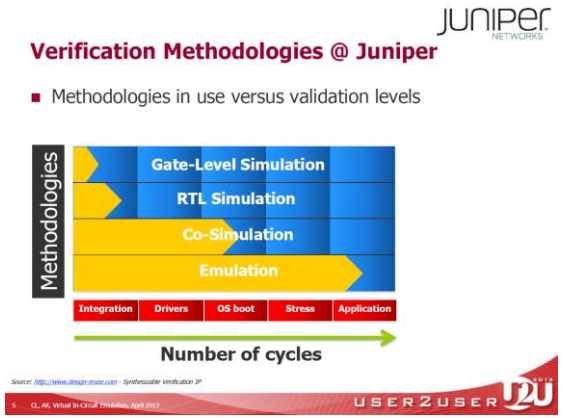
Driving new Emulation markets IoT, Automotive & Mil-Aero

Latest's Press Releases

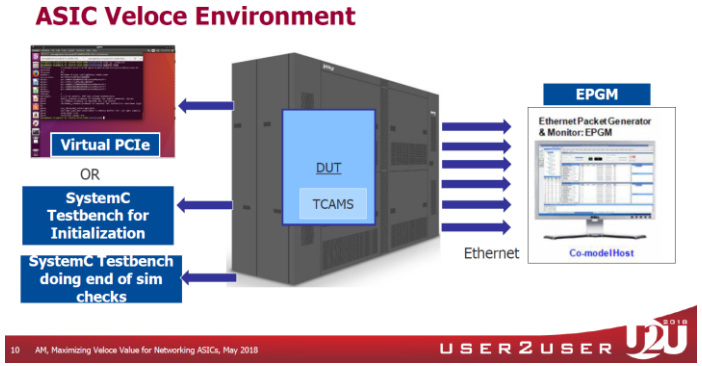
* Upon request the largest Veloce customer gates removed from count

Veloce for Networking Designs Customer Adoption

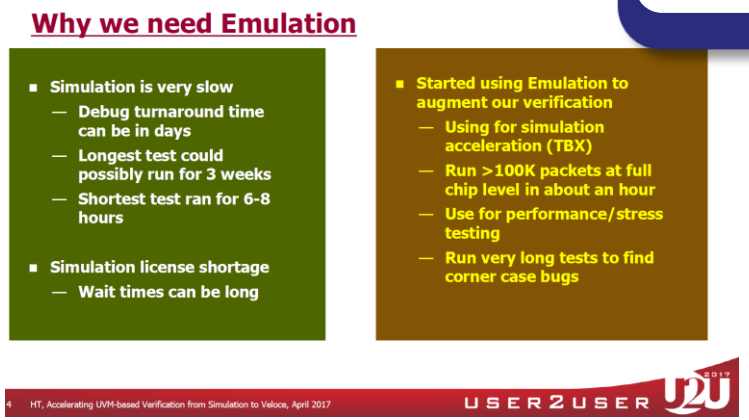
Networking



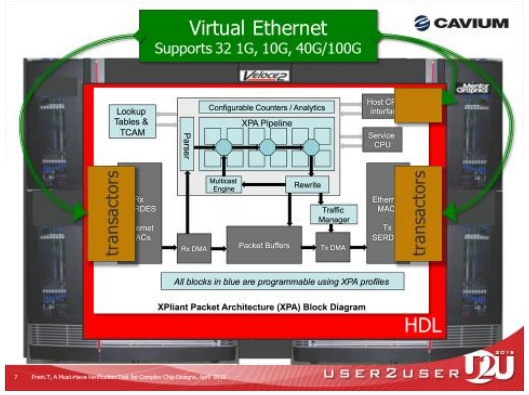
Juniper Networks



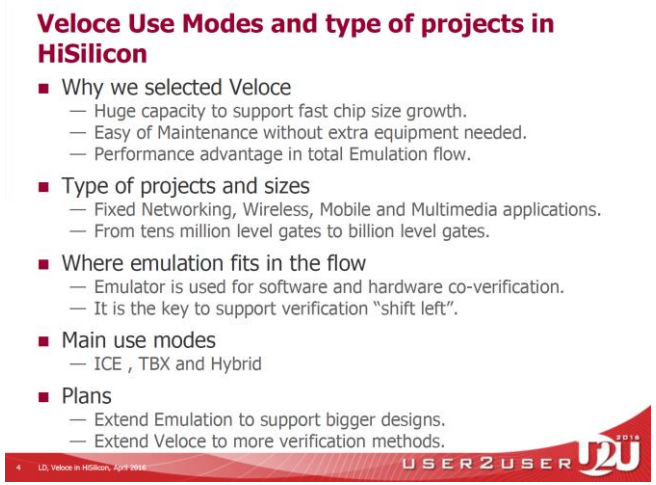
Cisco



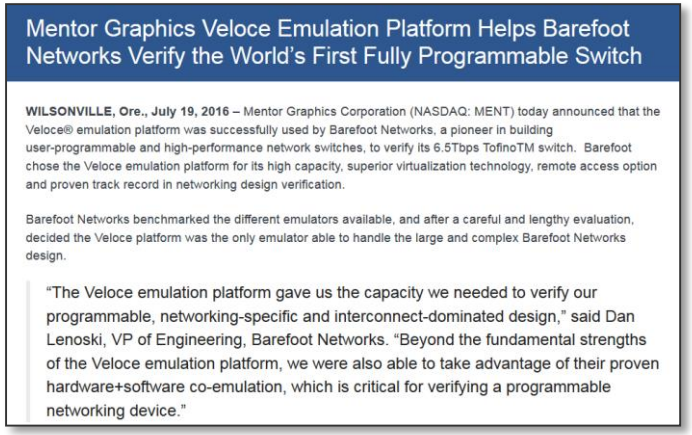
Palo Alto Networks



Cavium



Hisilicon



Barefoot Networks

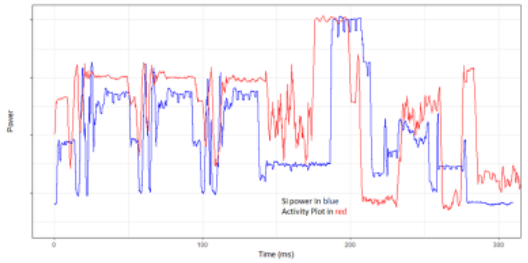
Mentor A Siemens Business

Summary : Leadership in Mobile, CPU/GPU, Networking and Storage

SAMSUNG

Comparison to Silicon Data (2/2)

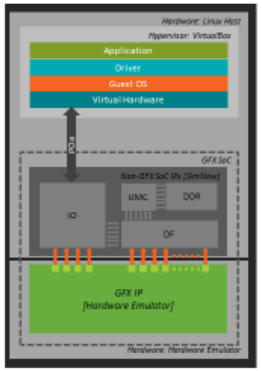
- Floating Point workload from Geekbench v4 suite
- Silicon data from prior generation
- Raw ActivityPlot data overlaid on silicon data
- Differences in magnitudes should not be interpreted as 'error'
- ActivityPlot CR=1024; silicon data 1ms granularity
- Further calibration of ActivityPlot data and debug of deltas are work in progress



USER2USER U2U 2018

AMD

SimNow™ Virtual Platform – Hybrid configurations



Hybrid Mode #3:

On Emulator: Graphics IP
In SimNow™: AMD GPU SoC
In VirtualBox: x86 Processors, Memory, and I/O

Benefits:

- Accelerate graphics IP verification and driver development
- Quickly start executing OS and system software, and graphics performance tests

14 TM, Multi-level modeling Techniques for pre-silicon, May 2018 USER2USER U2U 2018

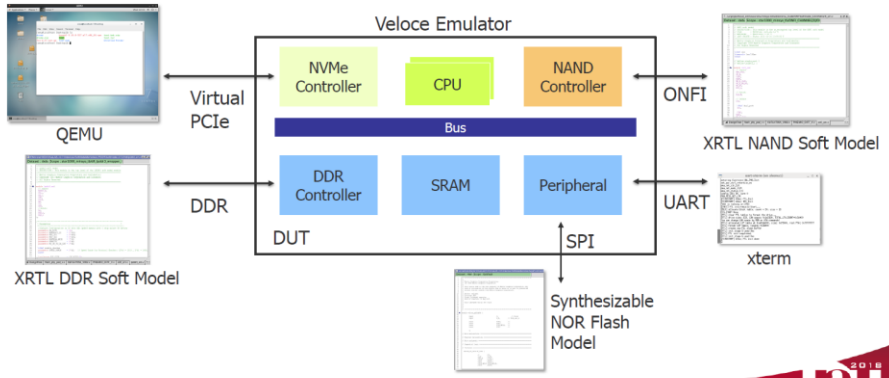
Performance Metrics - Packet Streaming

Simulation	Emulation
40 packets per minute	600000 packets per minute

Runs 15000X over simulation

17 AM, Maximizing Veloce Value for Networking ASICs, May 2018 USER2USER U2U 2018

Full Virtual Emulator Environment

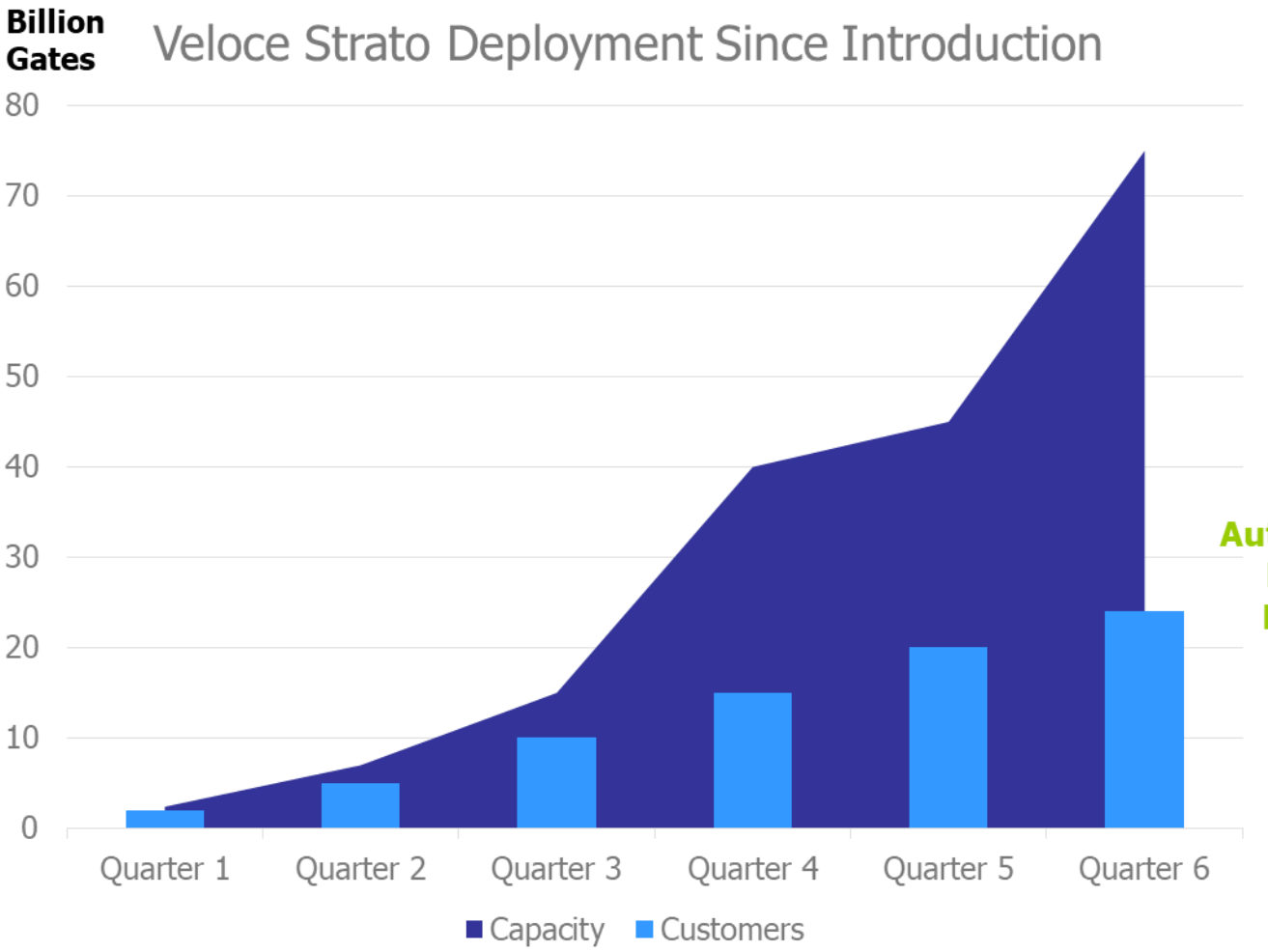


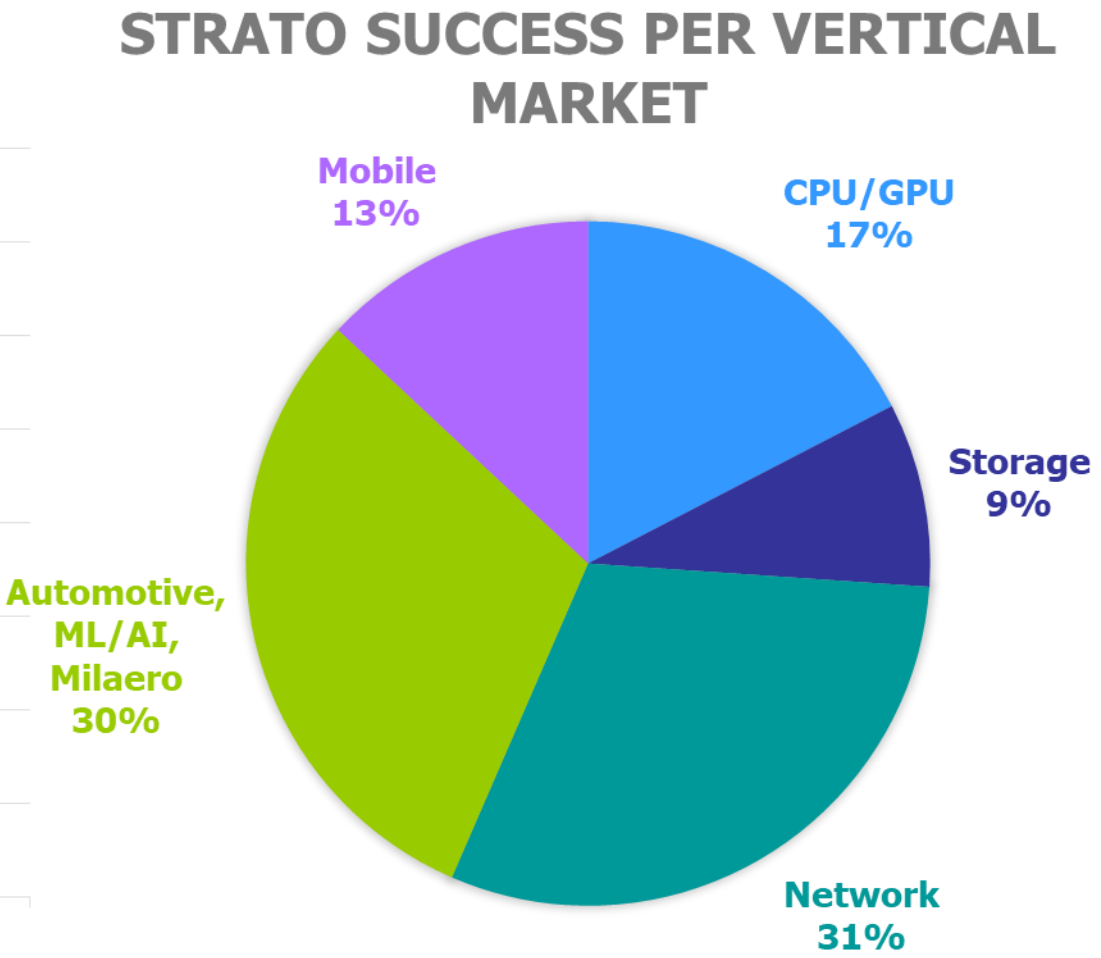
7 BC, Improve Firmware Design Schedule by Combining ASIC Simulator and Veloce Emulator, May 2018 USER2USER U2U 2018

STARBLAZE

Mentor® A Siemens Business

Veloce Strato: Customer Adoption



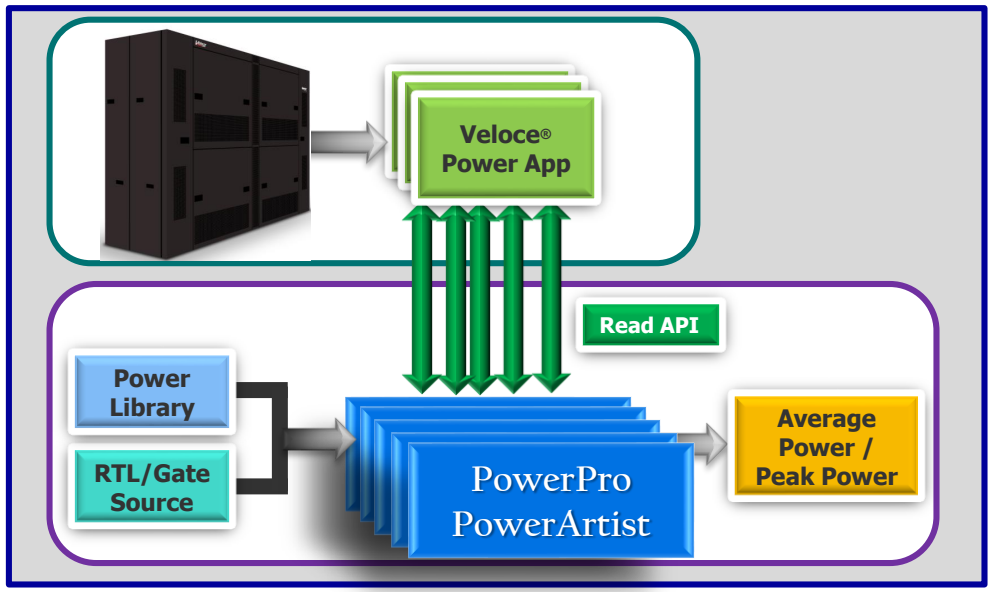


A Siemens Business

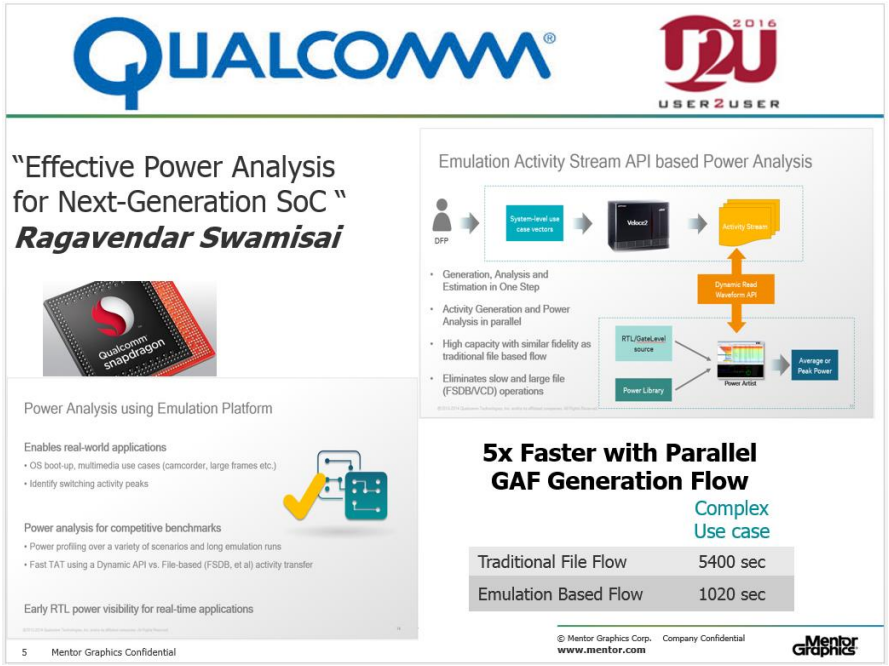
www.mentor.com

BACKUP

Veloce Power App: Fast and Accurate Power Analysis



- Average power
  - Read API
  - SAIF & SDPD SAIF for gate level netlist
  - FSDB
- Peak power
  - Read API
  - FSDB
- 10X Speed up over "FSDB based flow"



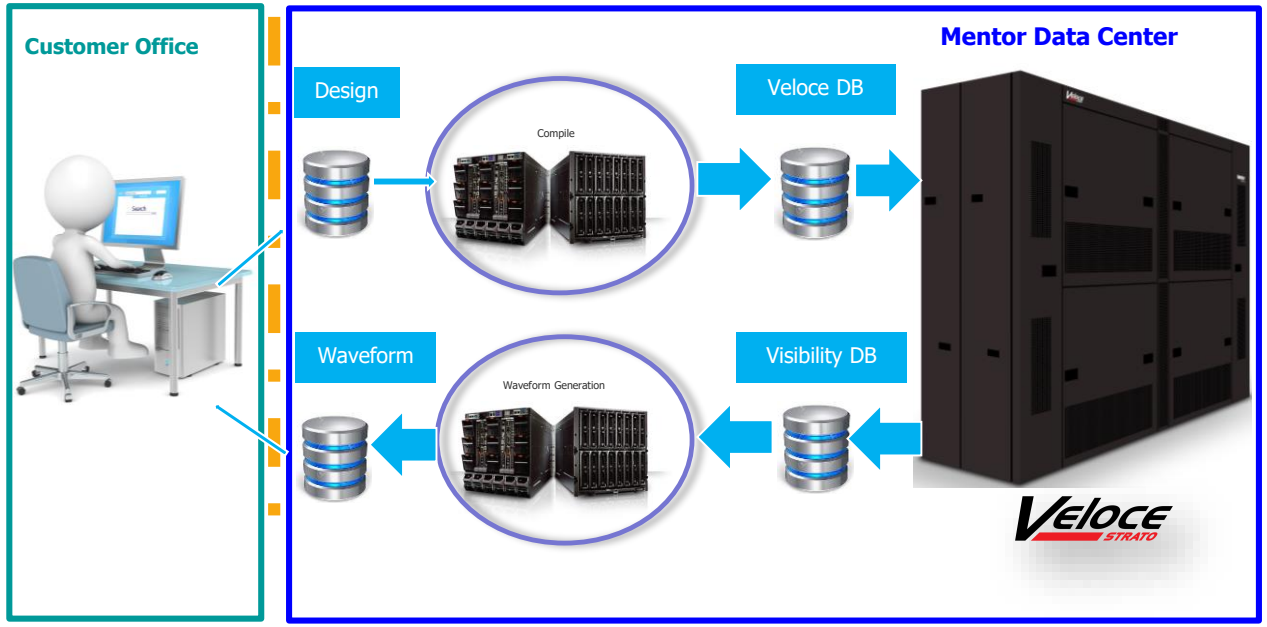
Design	Size	# Cycles	FSDB Flow	API Flow	X Factor
PCI Subsystem	42MG	11M	40 hours	5 hours	8x
Processor	65MG	15 M	51 hours	6 hours	8.5X
Video Enc-Dec	35MG	72 M	90 hours	8.5 hours	10.5x

Mentor® A Siemens Business

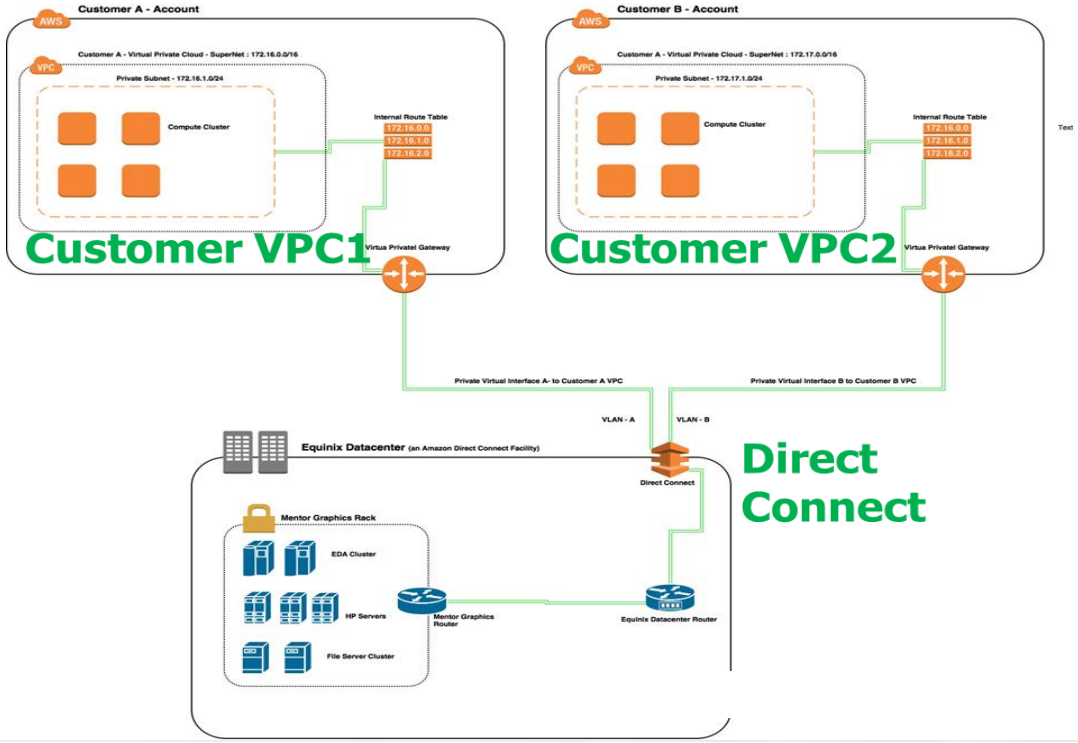
VELOCE
CLOUD HOSTING OPTIONS

Flexible Business Models incl Remote Usage

- Remote Usage – Mentor Cloud



- Remote Usage – AWS Cloud

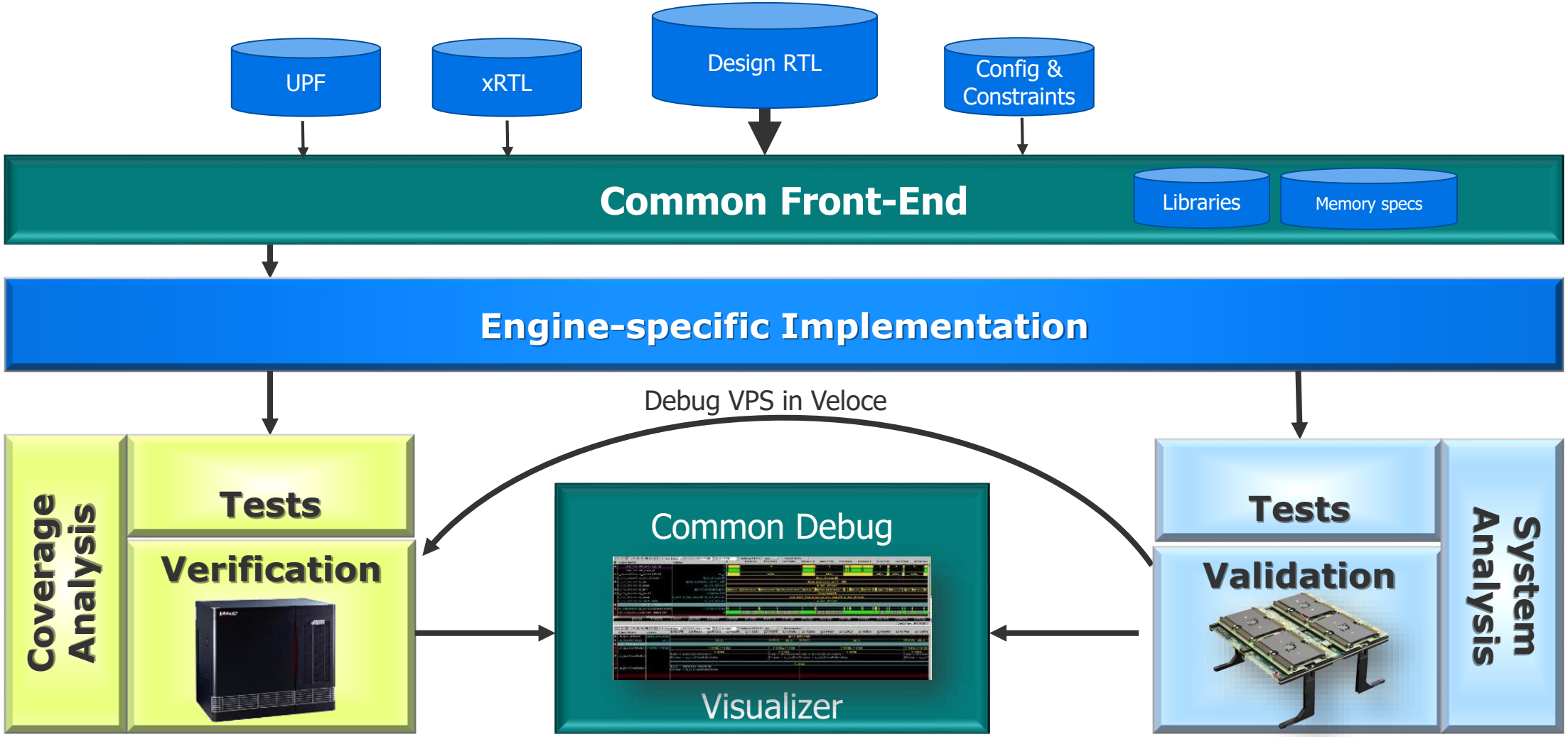


Seamless – Extended Customer Network
Fully Secure and Physically Locked in a Cage
Hassle Free Usage – No Addn'l Maint/Operation Expense

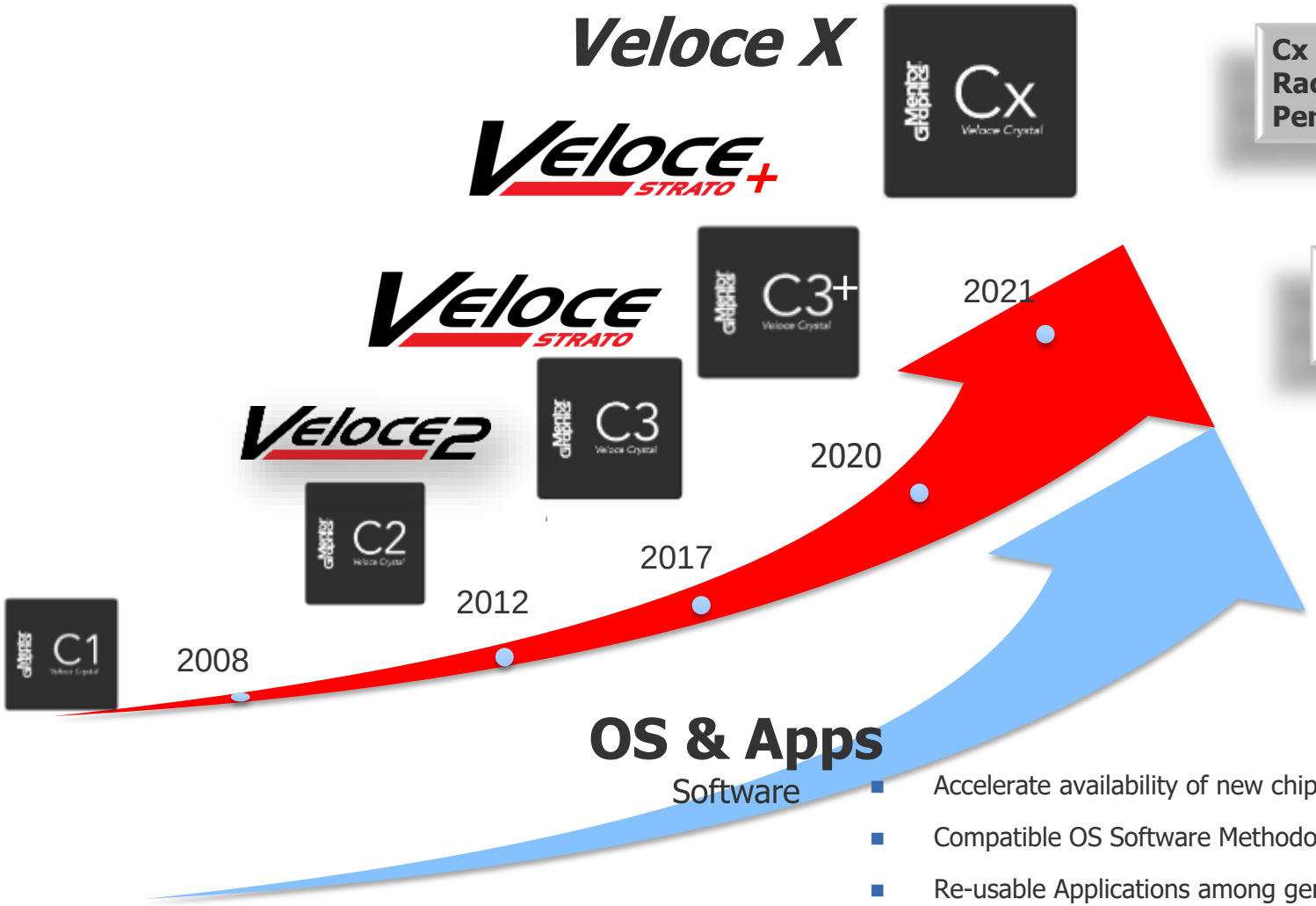
Fast – Efficient data transfer
Fully Secured by AWS on full transfer channel
Hassle Free Usage – No Addn'l Maint/Operation Expense

Mentor® A Siemens Business

Veloce and Prototyping Flow Compatibility



Funded Custom Chip and HW Roadmap



- Accelerate availability of new chips
- Compatible OS Software Methodology among generations
- Re-usable Applications among generations
- Re-usable Veloce Solutions