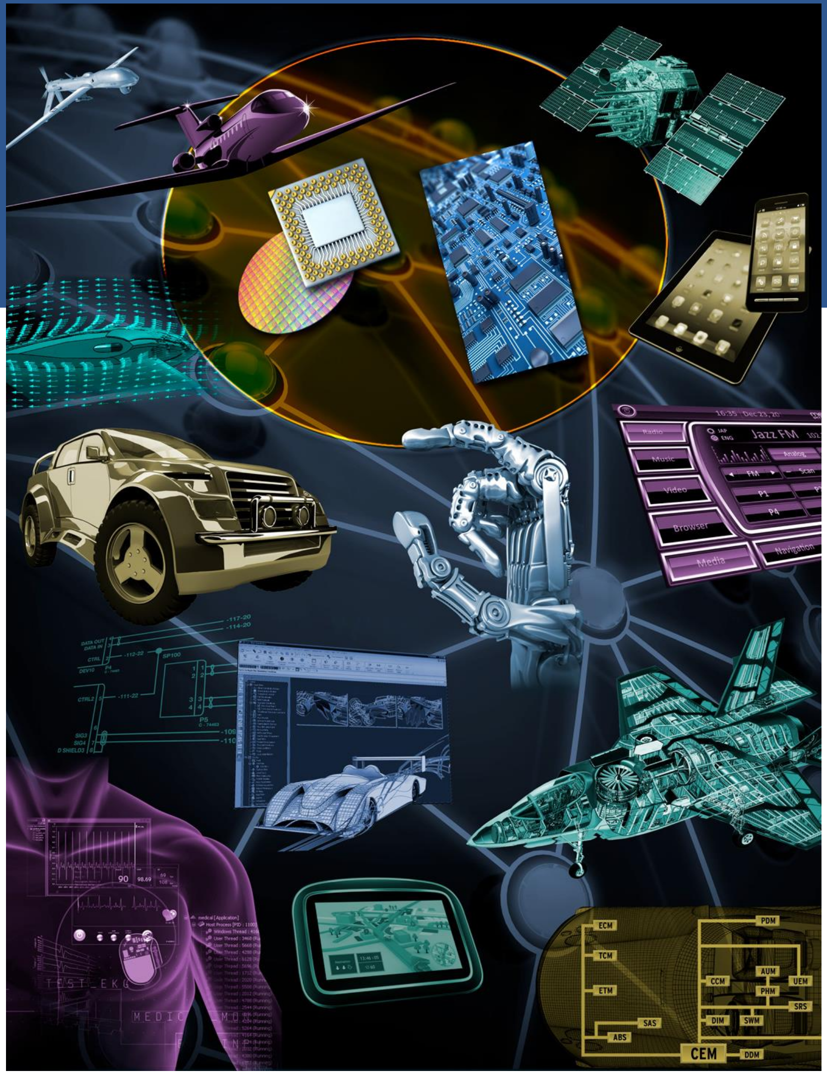
Tanner EDA Solutions General MEMS Overview



Mentor®
A Siemens Business

Региональный менеджер Mentor Graphics в России

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+7 916 323 9821
Москва, Шаболовка 10

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Corporate Overview & History

SIEMENS

Ingenuity for life

- Tanner EDA solutions have been in the market since 1988, 30 years.
- Widely used for analog/mixed-signal ICs and MEMS.
- 1,000+ of customers in 67 countries
- Tanner EDA was acquired by Mentor Graphics March 3, 2015
- Mentor joined Siemens in February, 2017

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Worldwide Locations

Tanner EDA Solutions Overview

Analog/Mixed-Signal IC Design

- A complete analog & mixed-signal IC design environment in one highly-integrated end-to-end flow

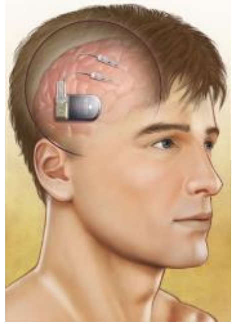
MEMS Design and Modeling

- Tanner EDA offers proven, powerful MEMS tools from mask design to 3D model creation for visualization and export to FEM analysis and MEMS-IC co-simulation

- Internet of Things (IoT)
- RF Applications
- MEMS Design & 3D Modeling
- Automotive
- Life Sciences
- Sensors & IC
- Military, Aerospace, Space
- Power Management
- Imaging & Displays
- Consumer Electronics
- Industrial

How Tanner Tools Address IoT Designs

second SIGHT
www.2-sight.com



NEUROPACE

Proteus™

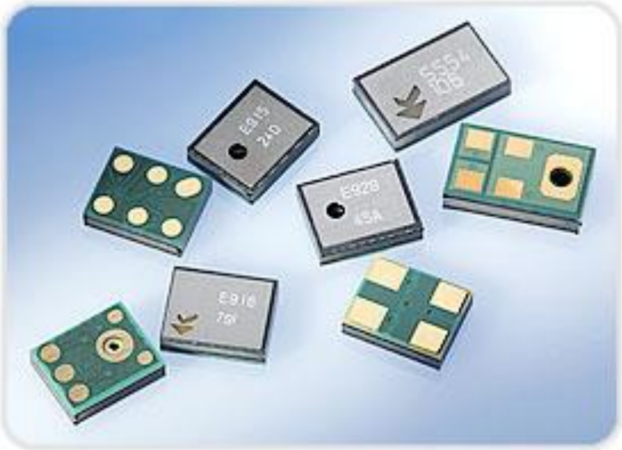
KNOWLES

- Top-down design of MEMS, analog, and digital in a single tool flow for all the design on a single die or multiple dies
- Co-design first level packaging of MEMS die and ASIC die
- The MEMS design tool leader with layout features for MEMS including true-curve support, 3D model creation, all-angle & equation based DRC, and co-simulation of MEMS and IC
- Support and PDKs from specialty foundries like X-Fab, TowerJazz, ON-Semi, and MEMS fabs

Breakthroughs with Tanner EDA

KNOWLES SHIPS 2 BILLIONTH SISONIC™ MEMS MICROPHONE

May 2011

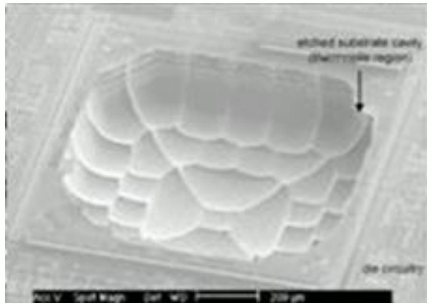


"With L-Edit, I can go from concept to finished GDSII in about two weeks. There's never been anything as easy to use as Tanner tools."

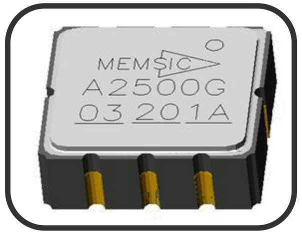
Pete Loeppert
Vice President R&D
Knowles Acoustics

Souvenir Olympic Torch by MEMSIC

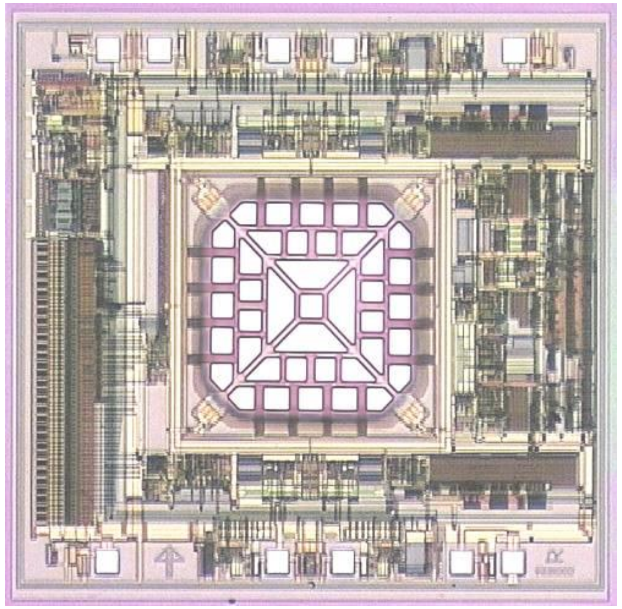
- Electronics and MEMS on the same die
- Low cost, high volume, low size, low power

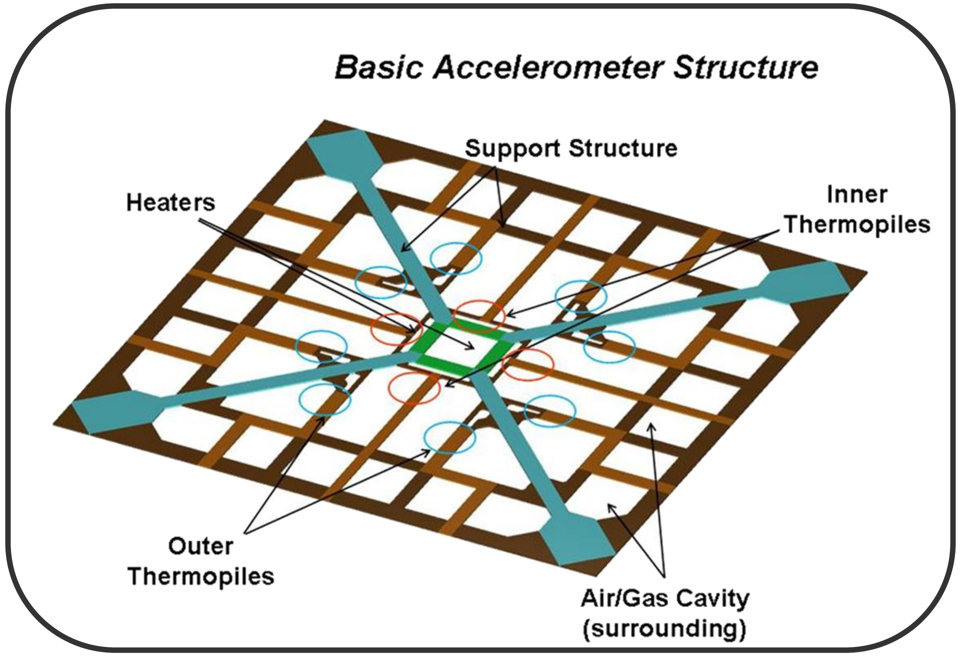


Olympic Torch in Action



Accelerometer Chip

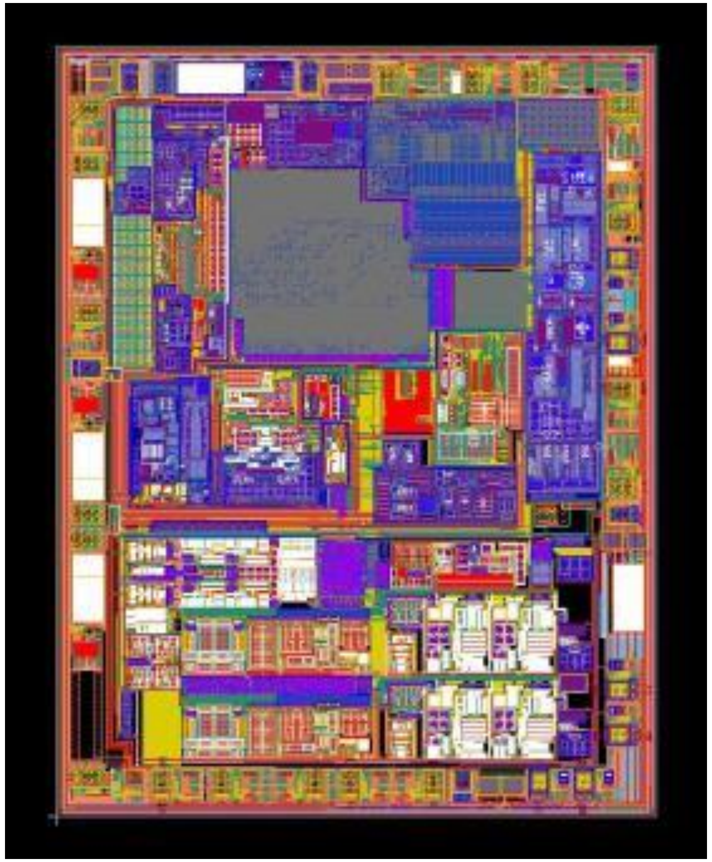




Images courtesy of Yongyao Cai, Director, Technology Partnership and Development, MEMSIC, Inc.

Combining Techniques – TPMS Sensor

- Single die handles analog, ADC, power management, digital control, and RF
- Co-designed with MEMS pressure sensor, combined into a single IC package
- Only external components are passives, battery, and antenna

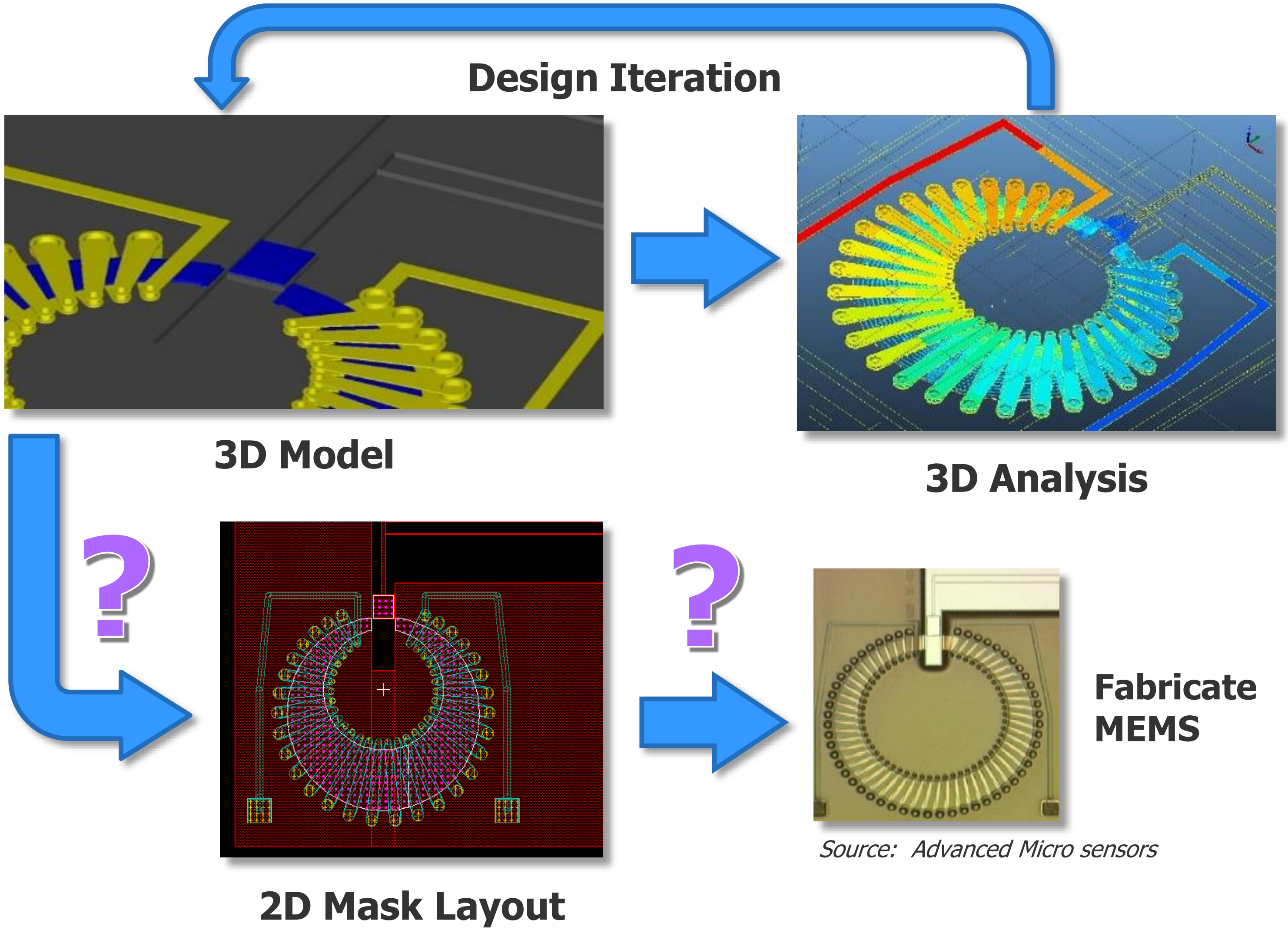


Source: Swindon Silicon Systems

MEMS DESIGN FLOW

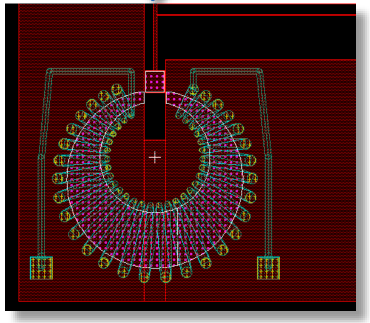
Design Flow - Other MEMS Tools

- How Can I Get 2D Layout Masks From My 3D Model?
- How Can I Be Certain My Layout Masks Will Fabricate My 3D MEMS Structure?

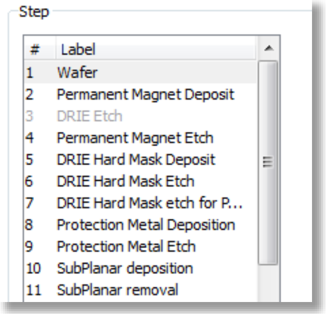


Design Flow - Tanner/SoftMEMS

Design Iteration



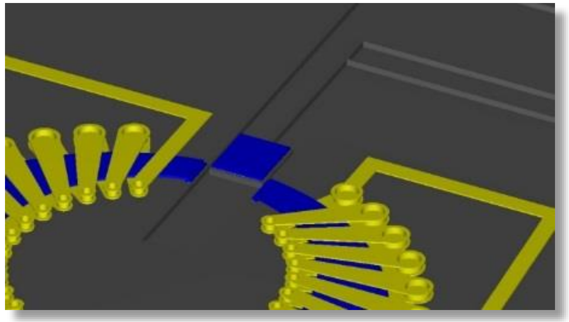
2D Mask Layout



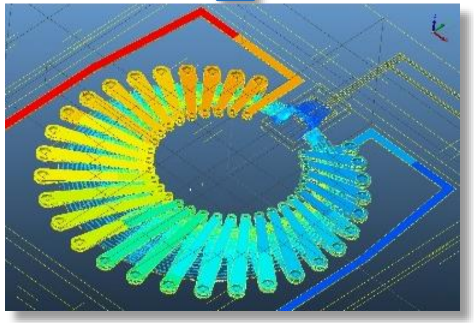
Step

#	Label
1	Wafer
2	Permanent Magnet Deposit
3	DRIE Etch
4	Permanent Magnet Etch
5	DRIE Hard Mask Deposit
6	DRIE Hard Mask Etch
7	DRIE Hard Mask etch for P...
8	Protection Metal Deposition
9	Protection Metal Etch
10	SubPlanar deposition
11	SubPlanar removal

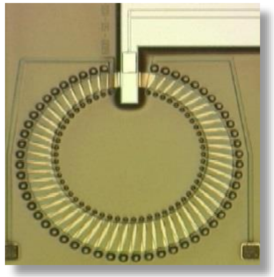
Fabrication Steps



3D Model



3D Analysis



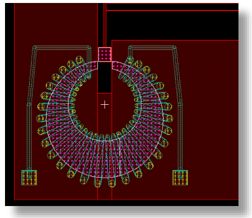
Fabricate MEMS

Source: Advanced Micro sensors

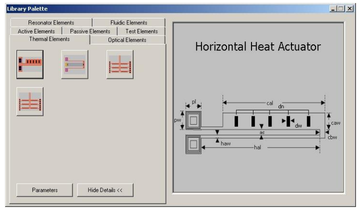
- Always Work From Layout Masks Which Are Used For Fabrication
- No Translating The 3D Model To 2D Layout Masks = Less Risk

MEMS Design Flow – Bottom-Up Methodology

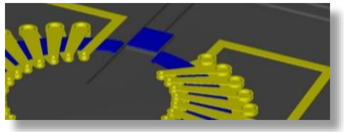
New Idea



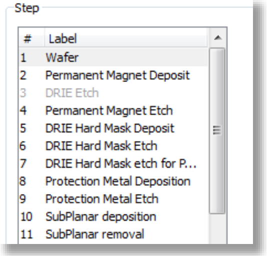
Draw Mask ← MEMS PCell Library

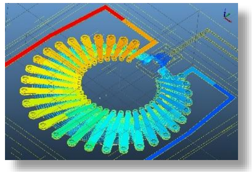


DRC



Generate 3D Model for FEM ← Process Info

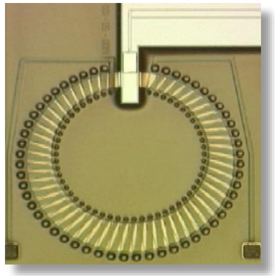




FEM/BEM

Compact Model Builder

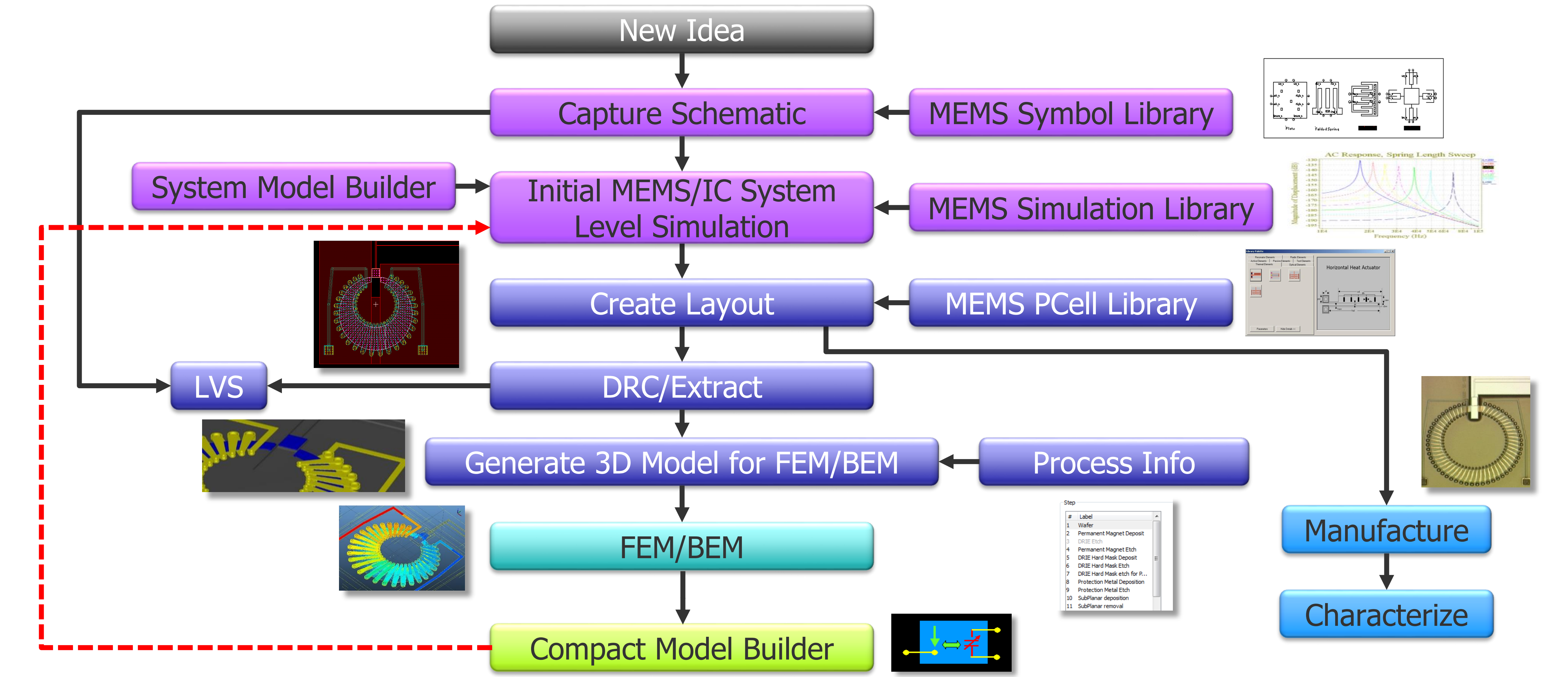
MEMS/IC System Level Simulation



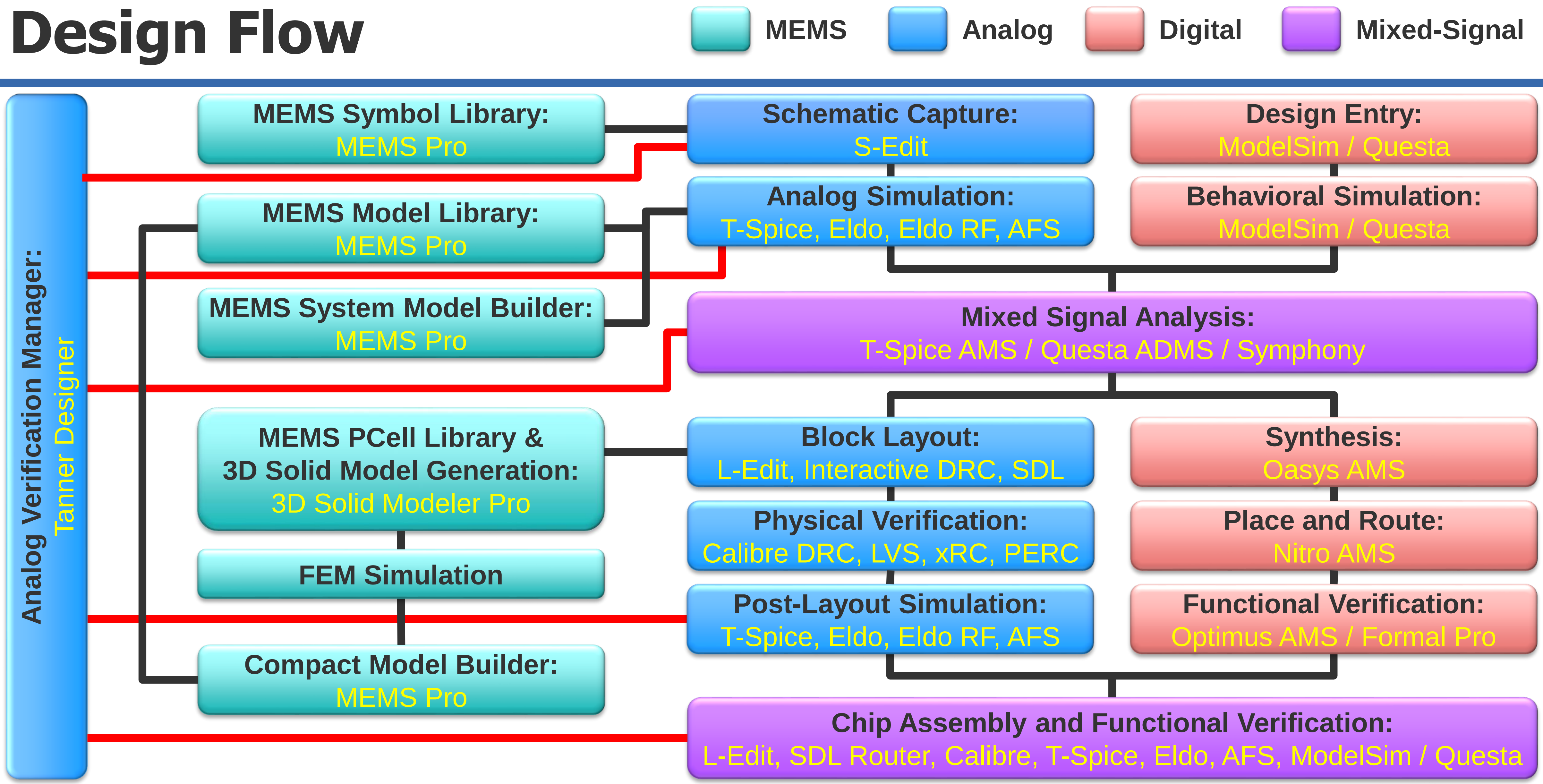
Manufacture

Characterize

MEMS Design Flow – Top-down Methodology



Design Flow



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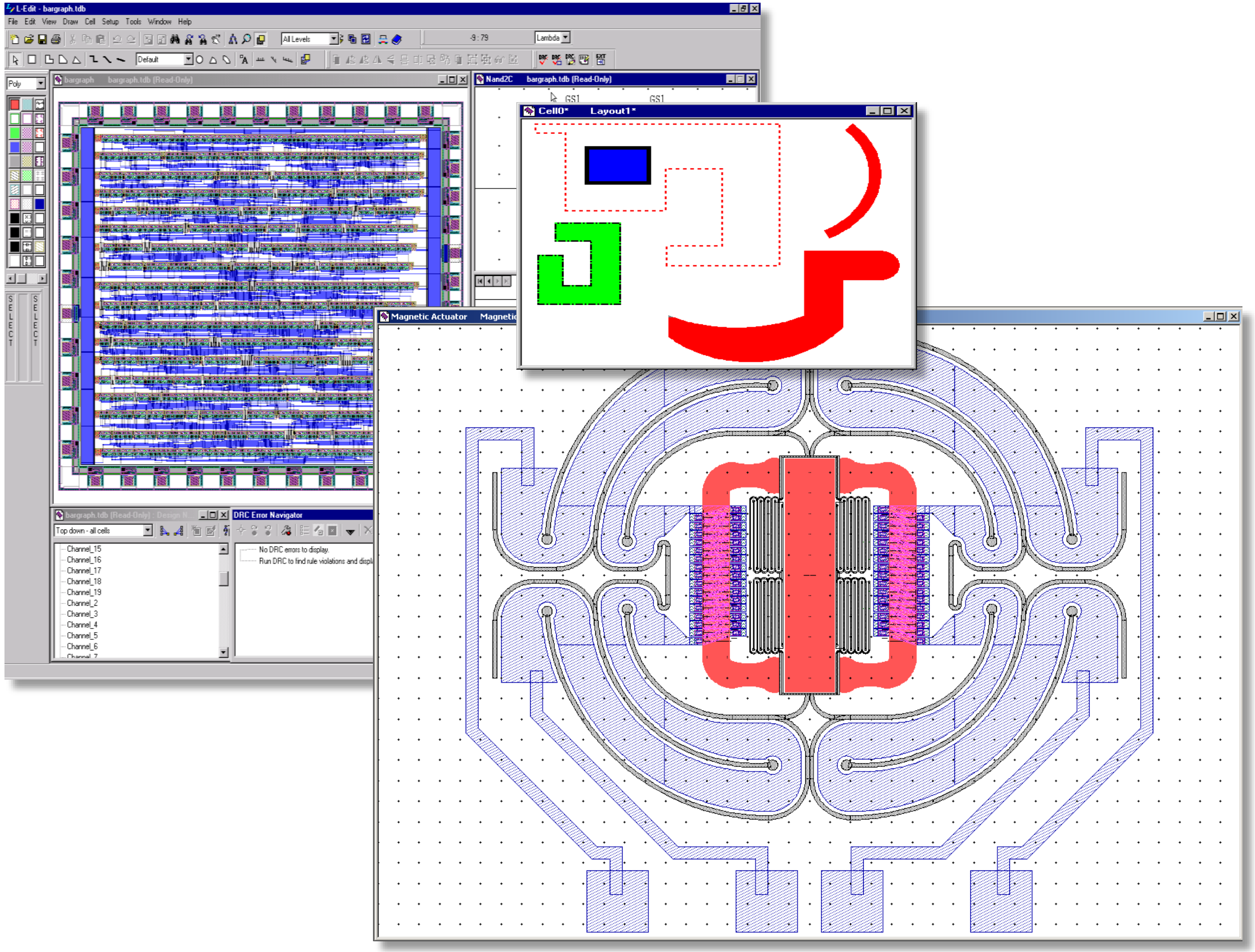
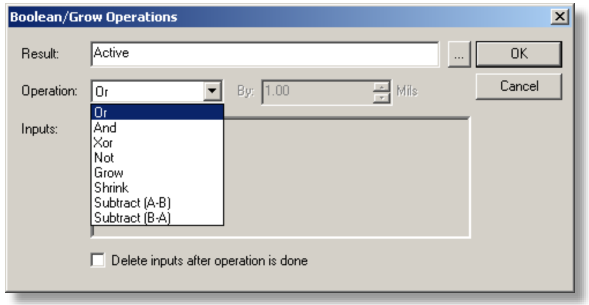
MEMS LAYOUT

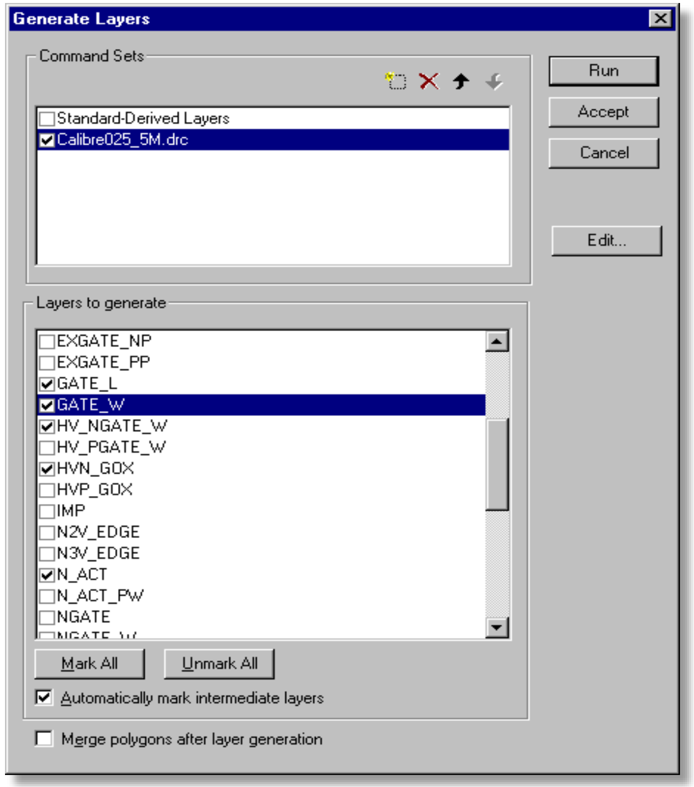
L-Edit MEMS – Full Custom All-Angle Layout Editor

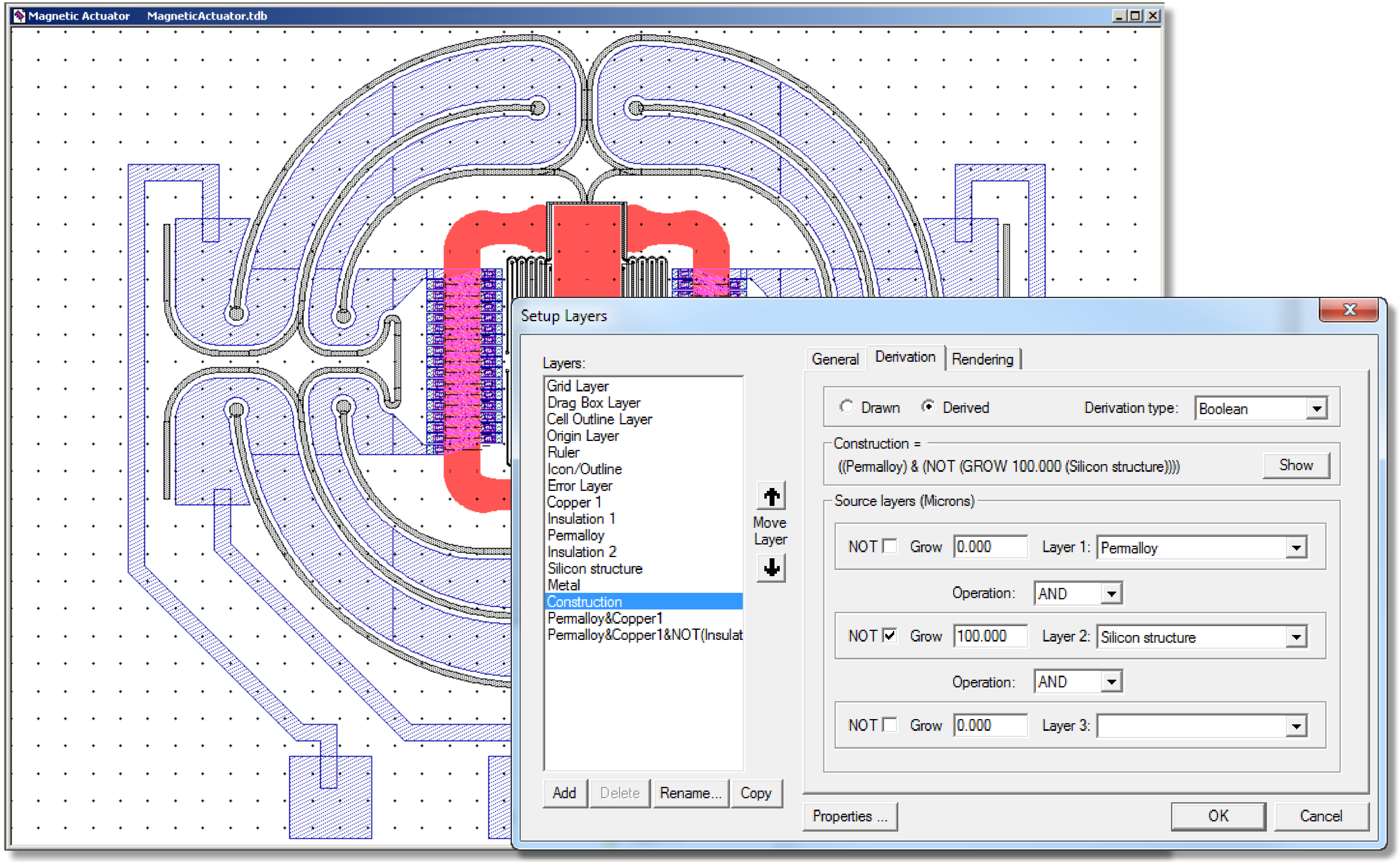
- The Only Tool Developed *Specifically* for MEMS *and* IC Design
- True Curve Support
- Technology Configurable
- Enhanced Boolean Operations
- Advanced Editing Support:
  - Object Snapping
  - Base Point
  - Alignment
- GDSII, CIF, EPS & DXF support
- Programmable Interface



L-Edit - All-Angle Generate Layers

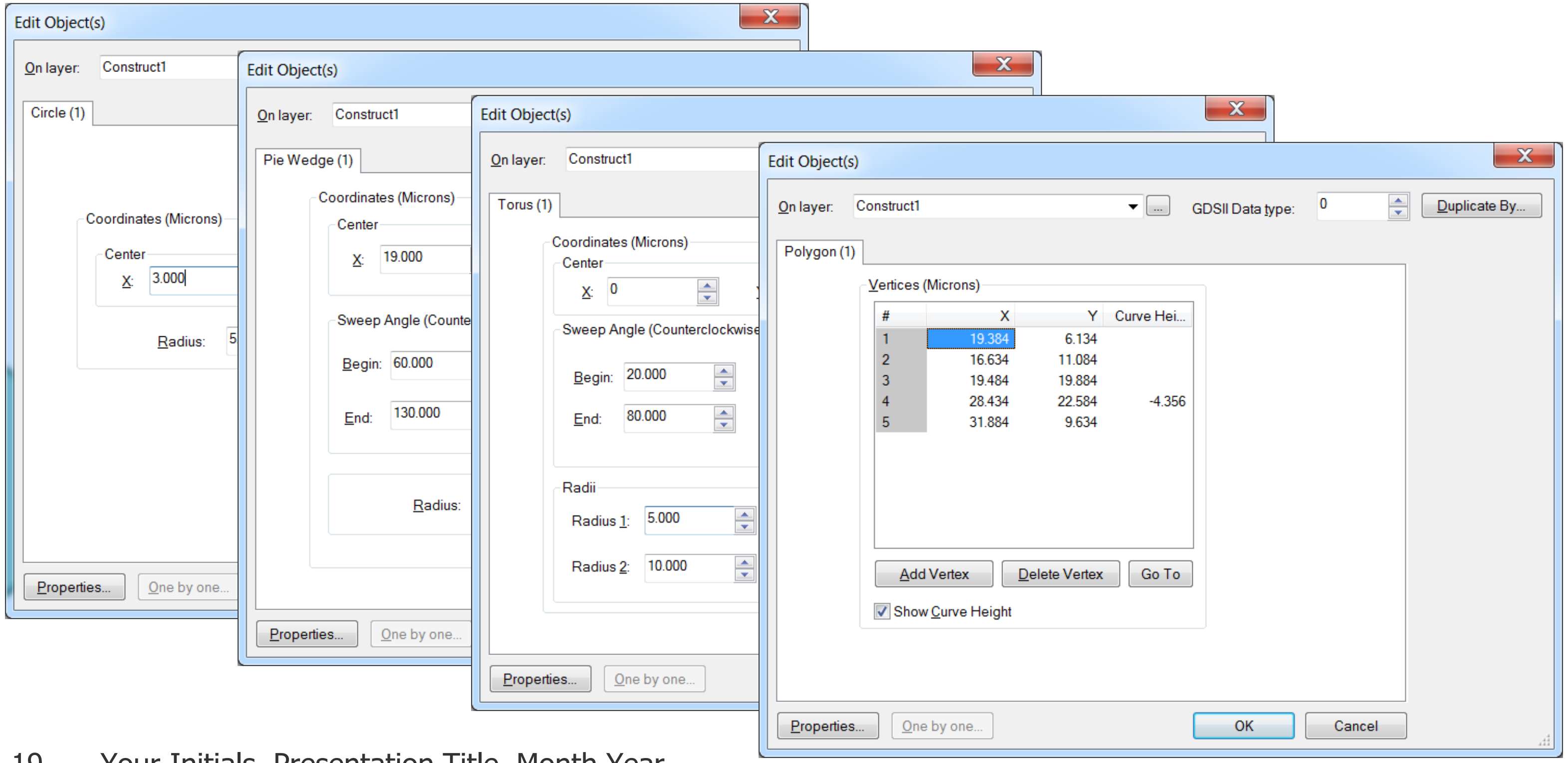


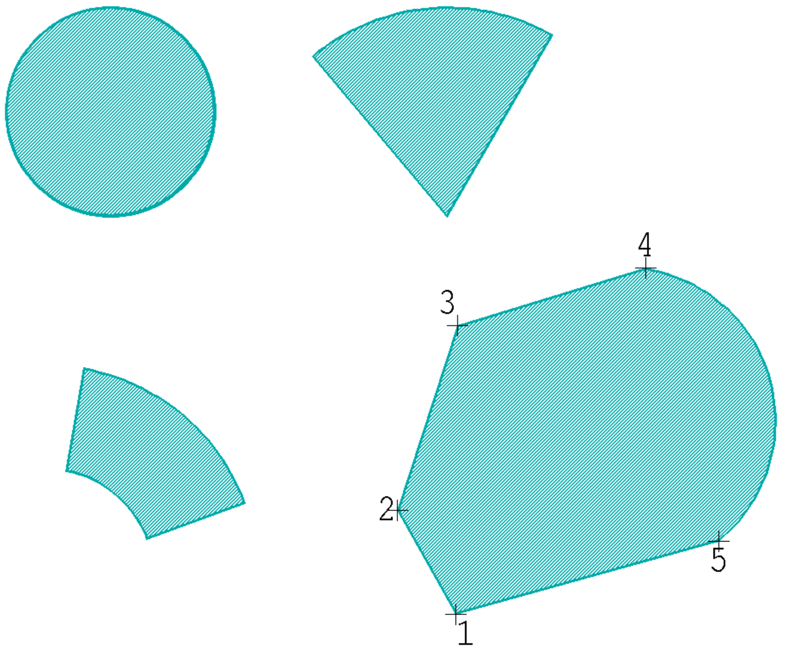




Curve Representations

- True Curved Polygon Representation
- Curved Object Types
- Graphical Editing Comparable With AutoCAD
- Textual Editing Of Curves





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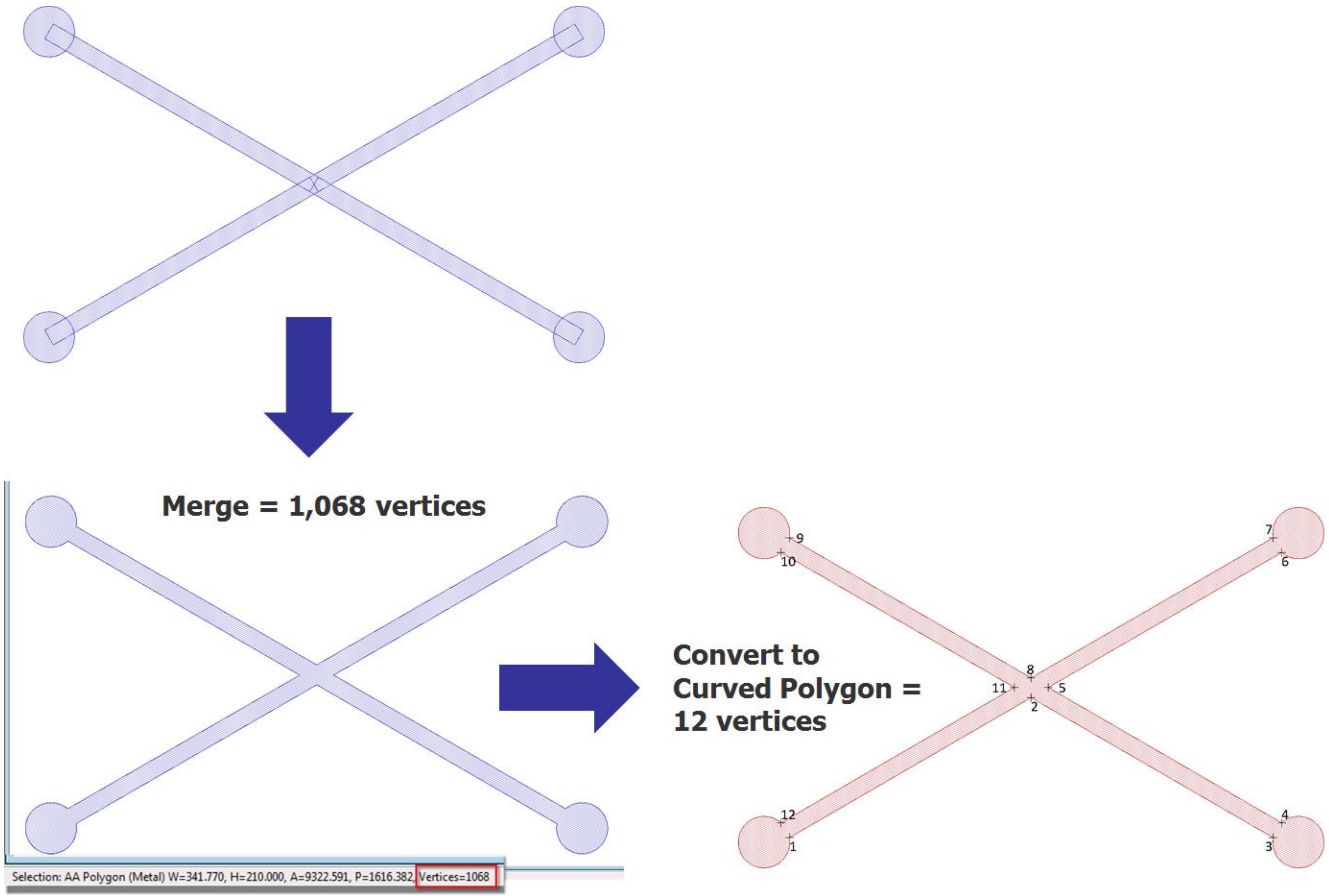
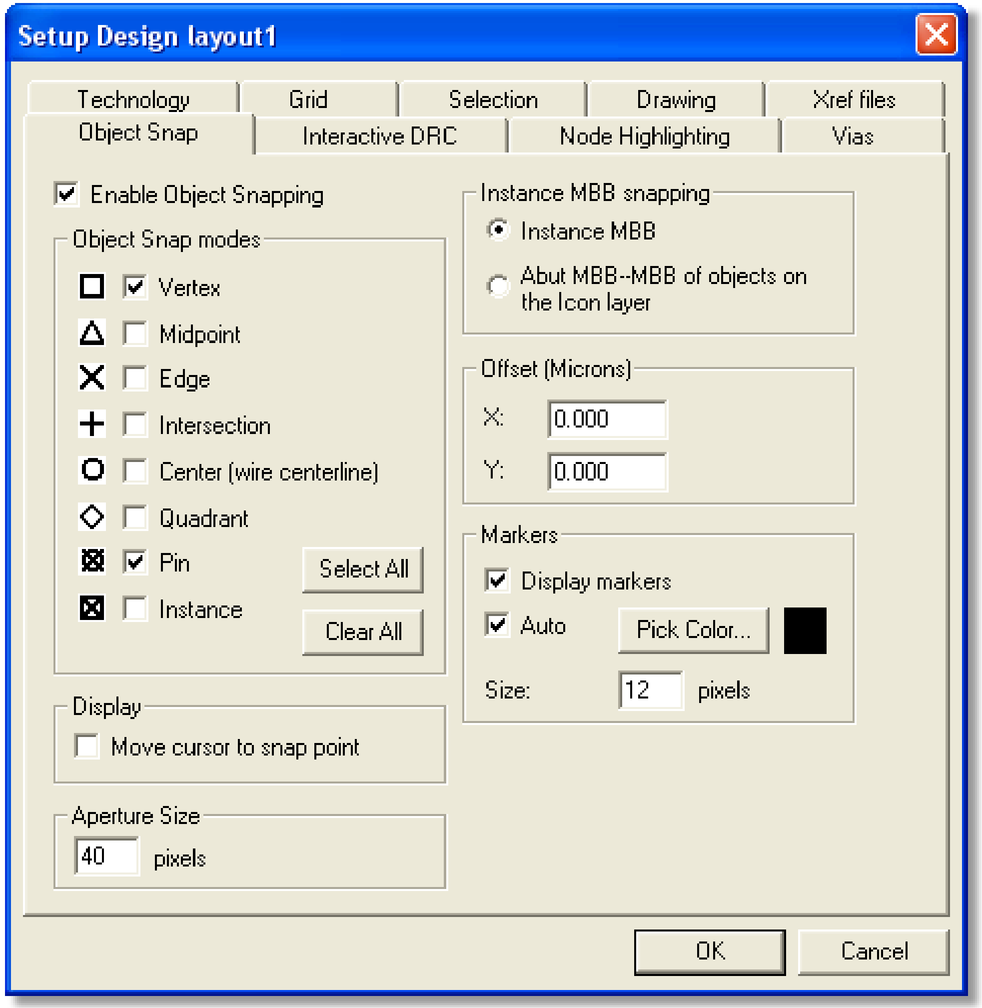
Reconstruct Curves From All-angle Edges

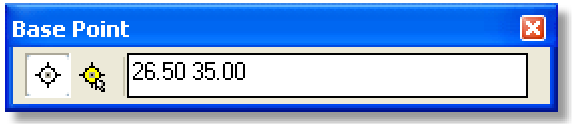


L-Edit – Object Snapping and Basepoint

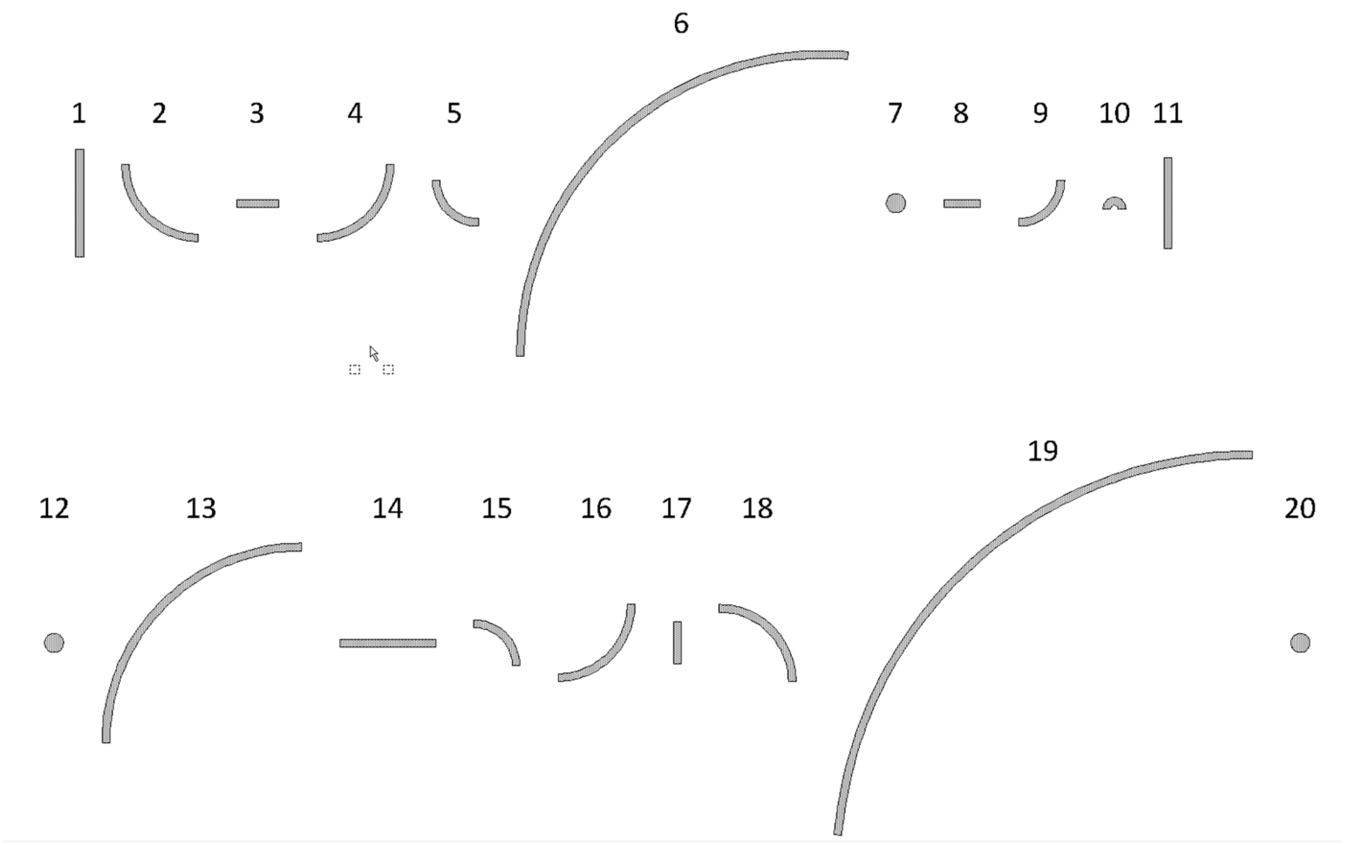
- Snap cursor to object features
  - vertex
  - midpoint
  - edge / centerline
  - intersection
  - center
  - pin (port on instance)
  - instance

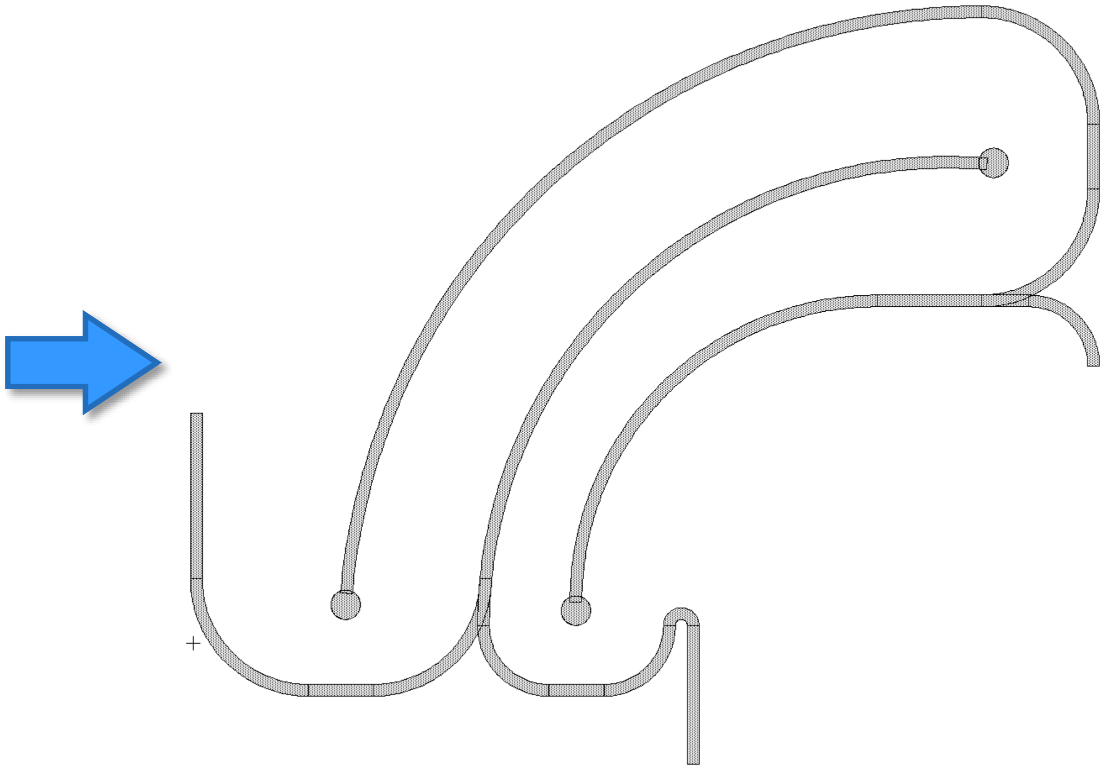


- Base Points for Precise Positioning

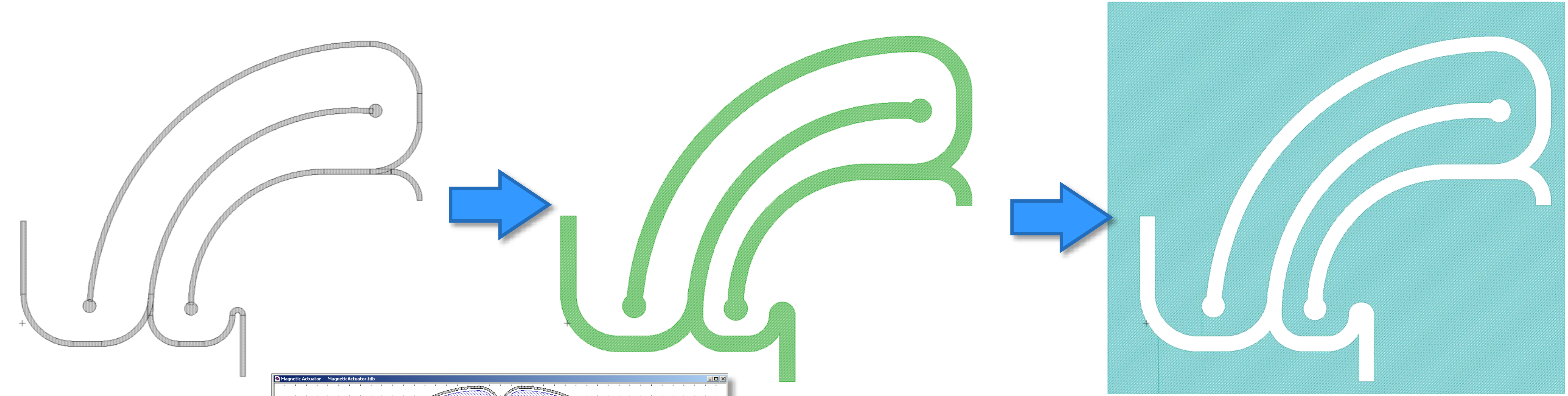


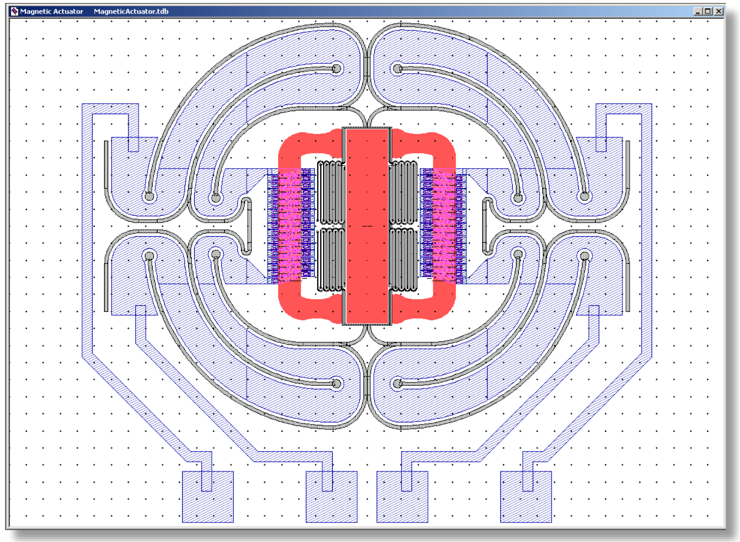
Complex Construction





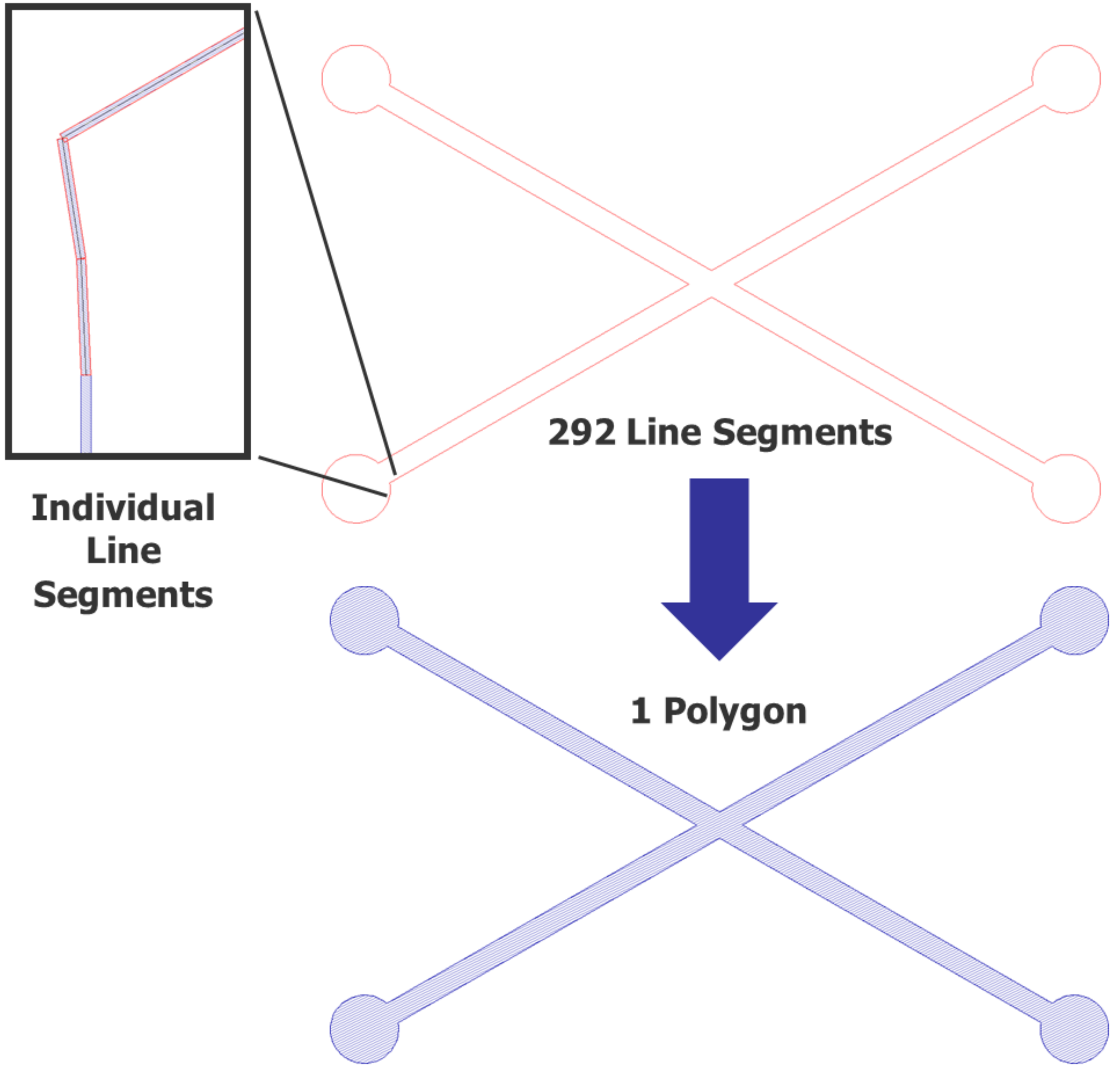
L-Edit - All-Angle Generate Layers





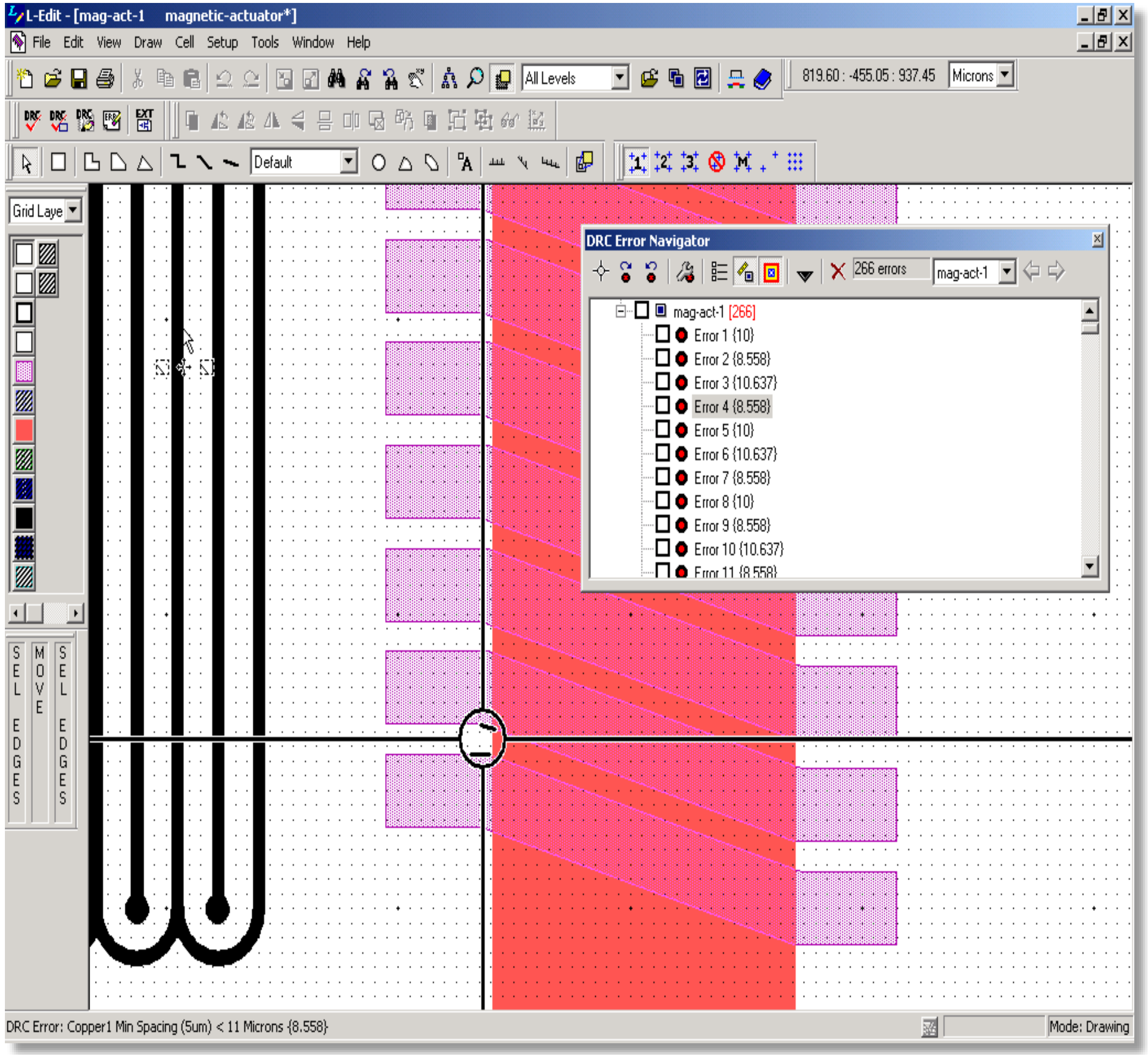
DXF Import/Export

- DXF Import With Boundary Reconstruction
  - Some CAD Tools Fracture Polygons Into Edges During Export
  - Connects Adjoining Edges Within A Tolerance Together Into A Filled Polygon
  - Can reconstruct curves from a series of all-angle edges



L-Edit - DRC for MEMS

- All Angle Design Rule Checking
- Check for minimum spacing between any type of polygonal objects on various layers.
- Find design flaws immediately!
- Complex DRC rules can be created and customized to meet proprietary MEMS fabrication processes.
- Development and maintenance of technology files easily manageable.



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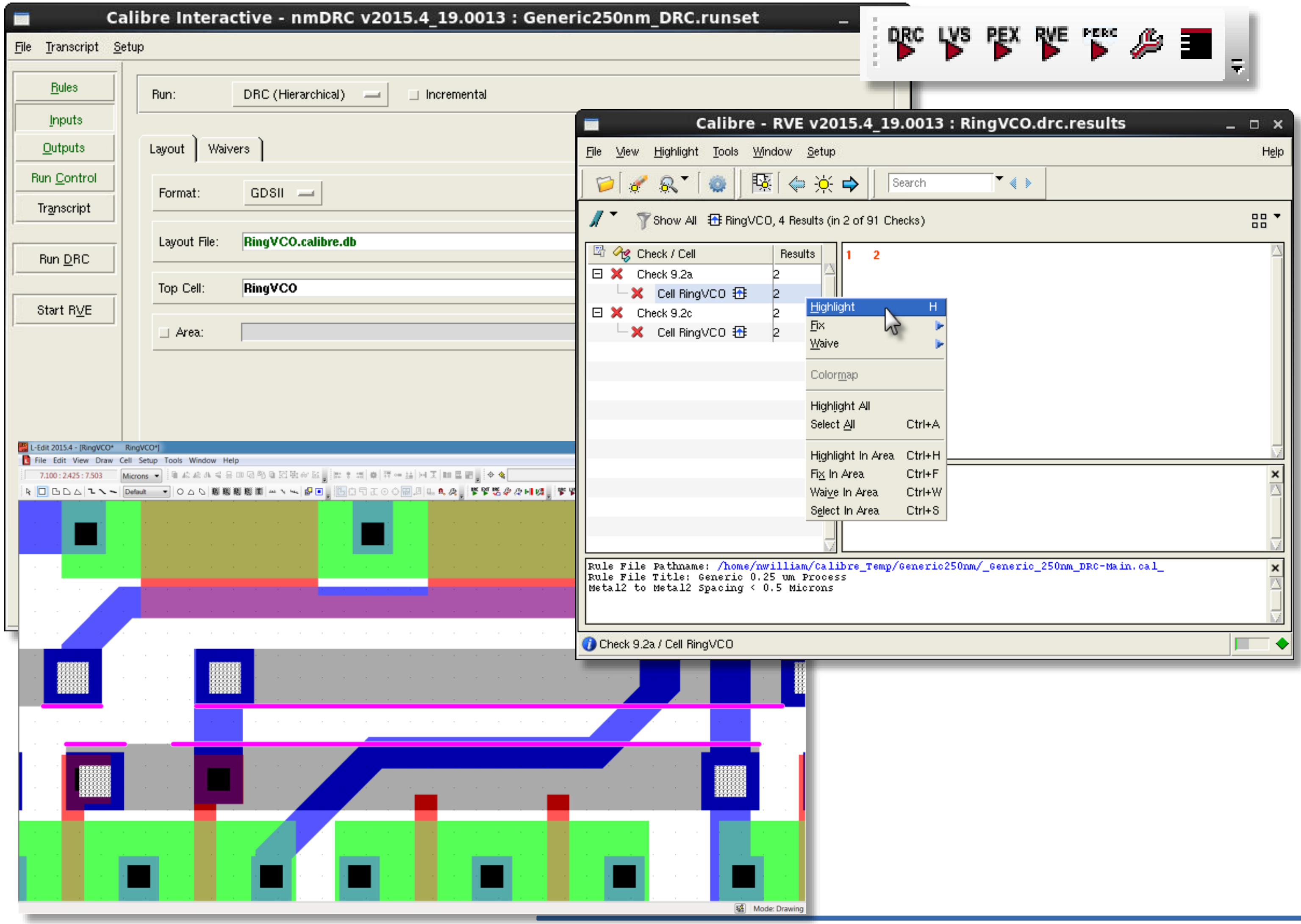
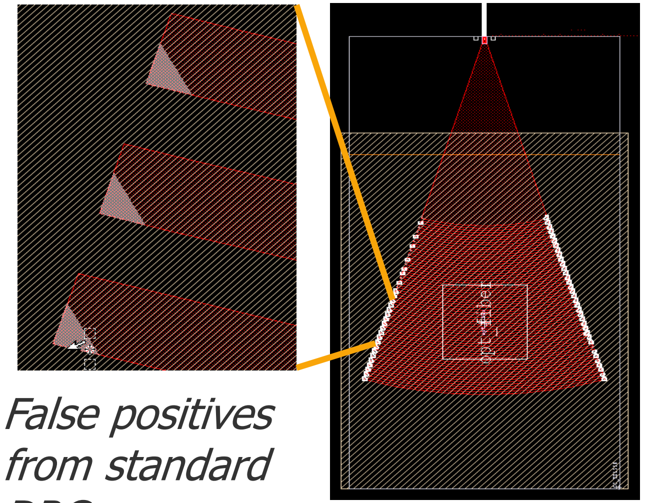
Tanner Calibre One

- Run Calibre nmDRC™ And Calibre nmLVS™ Directly From L-Edit
- Use Calibre RVE™ To View Calibre DRC, LVS, And PEX Results In L-Edit And S-Edit
- Access to equation based DRC (eqDRC) capability
- Foundry qualified signoff

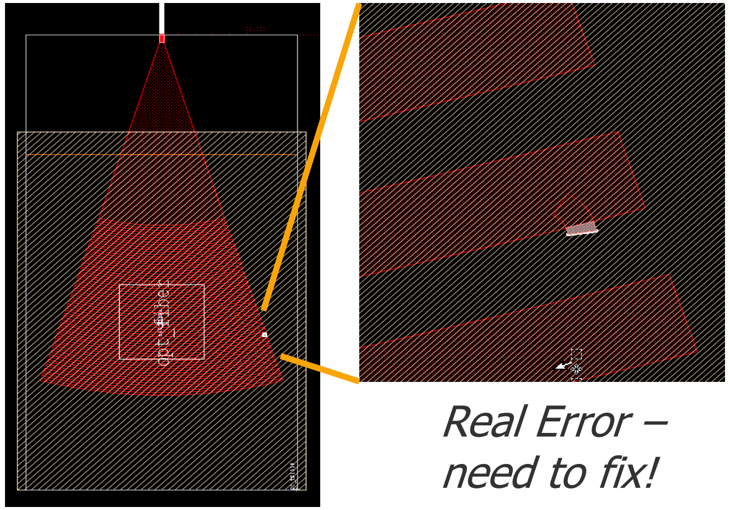


DRC

- Customary IC DRC rules produce large amounts of false errors in MEMS/Photonics designs
- False positive errors can mask the actual design error
- Equation based DRC (eqDRC) solves problem
- MEMS context sensitive rules
- Support device specific rules, e.g., fillets, mechanical rules
- Capture expert knowledge



False positives from standard DRC run

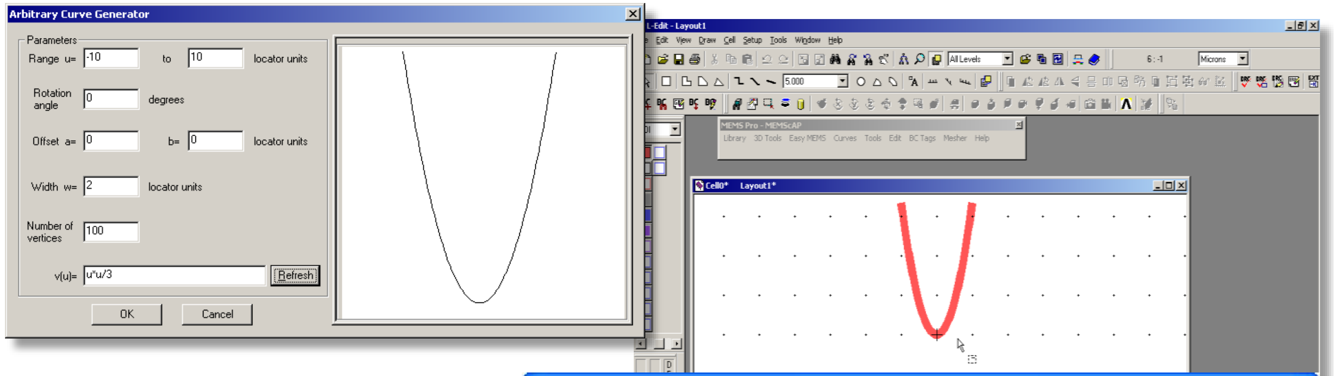


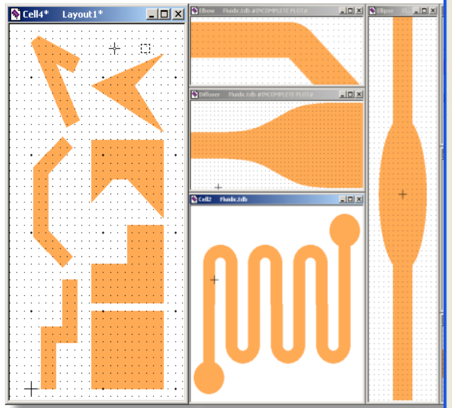
Real Error – need to fix!

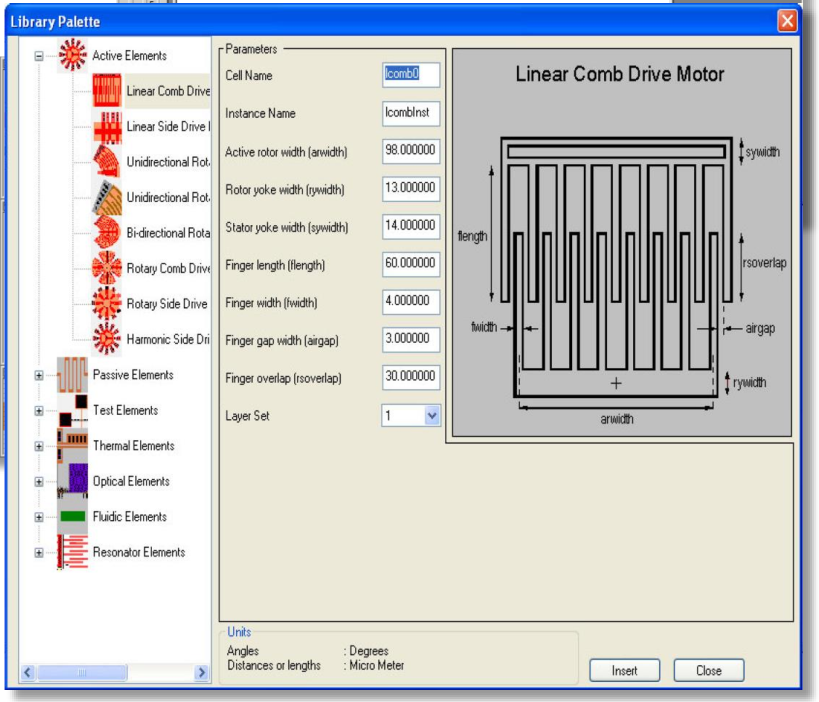
MEMS LAYOUT TOOLS

SoftMEMS Solid Modeler Pro

- MEMS toolbar
  - Arbitrary curves
  - Microfluidics and other MEMS technologies
- Easy MEMS
  - MEMS specific tasks such as adding release holes for Plates
- Library Palette
  - Basic layout generators for many MEMS devices creates layout you can use as a starting point and then modify for your specific design

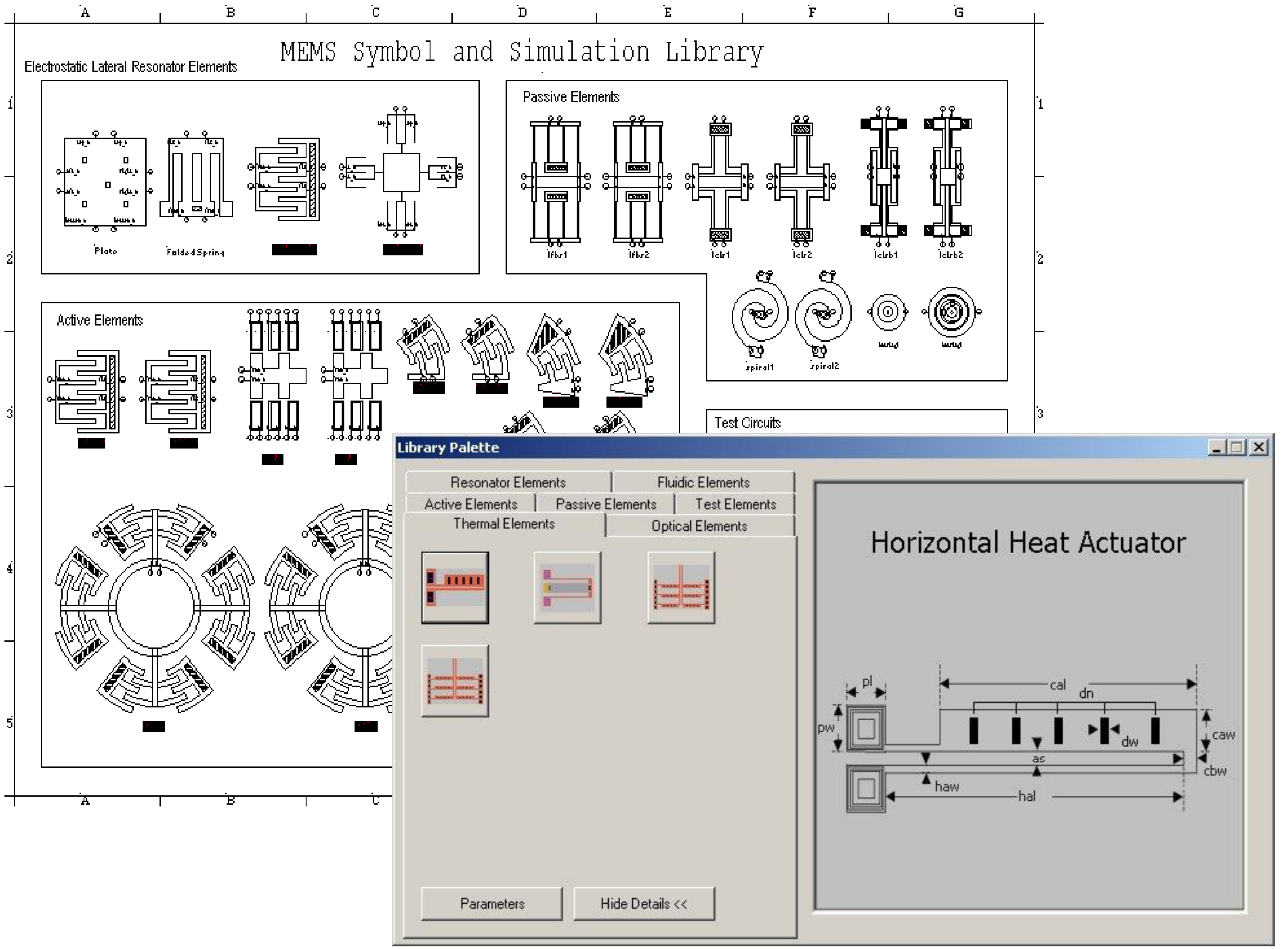






Libraries

- Supports SPICE, Verilog-A, VHDL-AMS, Matlab
- 3-View System of each component:
  - Schematic
  - Simulation models
  - Parameterized Layout
- Library creation by users with examples from us
- Important to encapsulate design rules in the library



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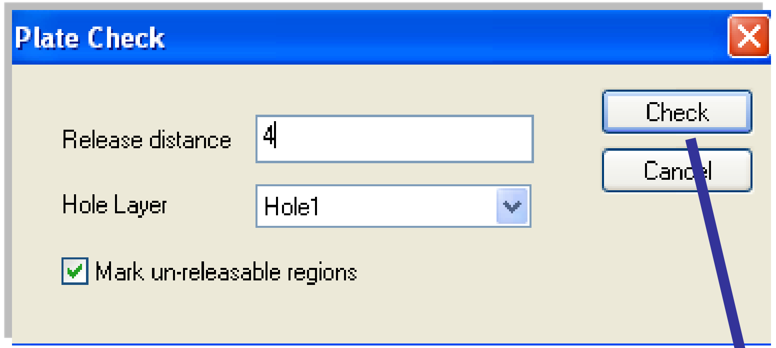
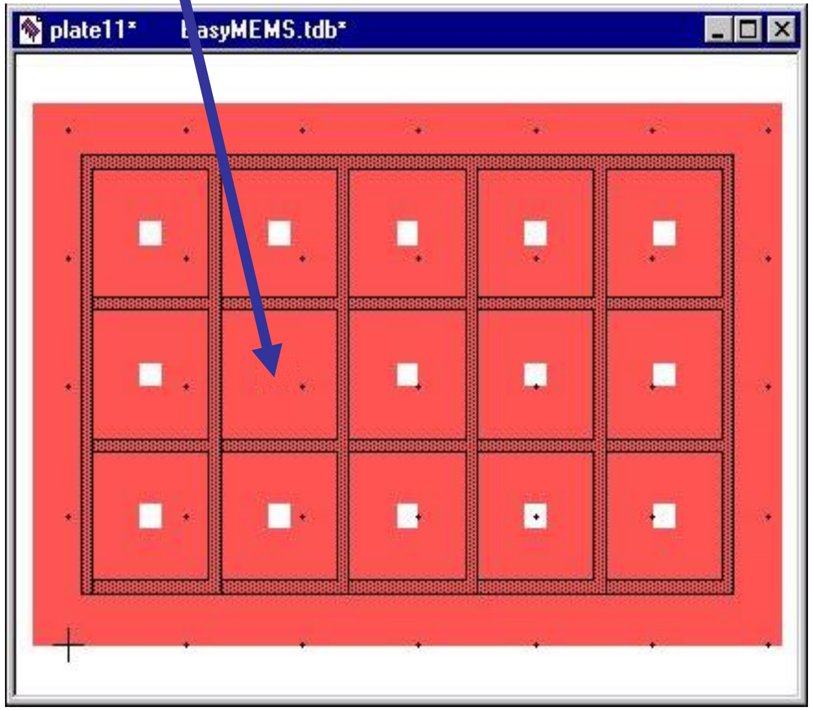
Design Rules and Guidelines

- DRC checks manufacturing rules, spacing, surround, size, etc.
- MEMS context sensitive rules
- Support device specific rules, e.g., fillets, pad rules
- Capture expert knowledge



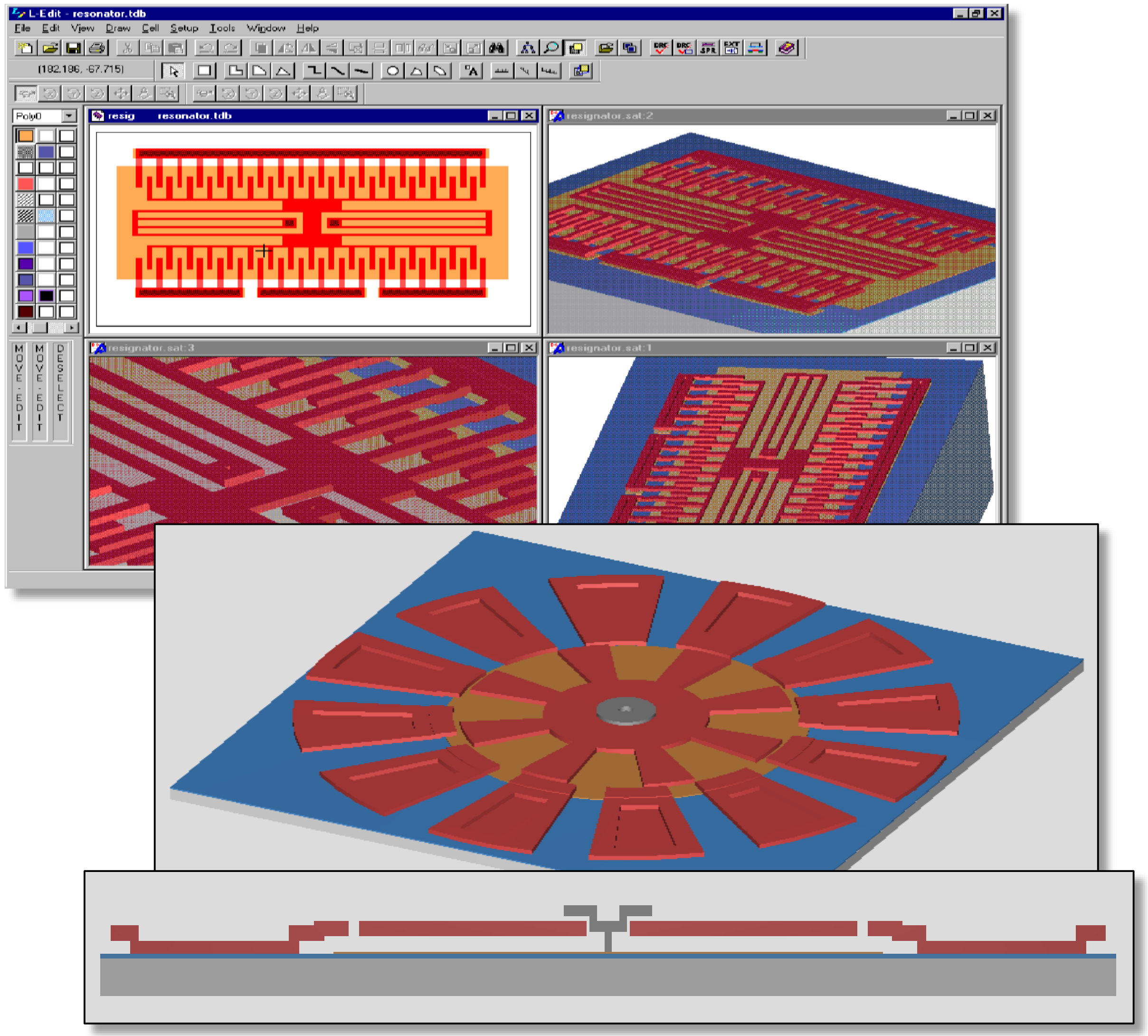
Unreleased regions marked on error layer



MEMS 3D TOOLS

Solid Modeling with SoftMEMS

- Create a 3D Solid model from masks and fabrication process description
- Gives 3D graphical representation of MEMS fabrication process
- Embedded in L-Edit
- Multiple views and cross-section
- Snapshot of model can be output
- Output may be sent to FEM/BEM programs for 3D Analysis



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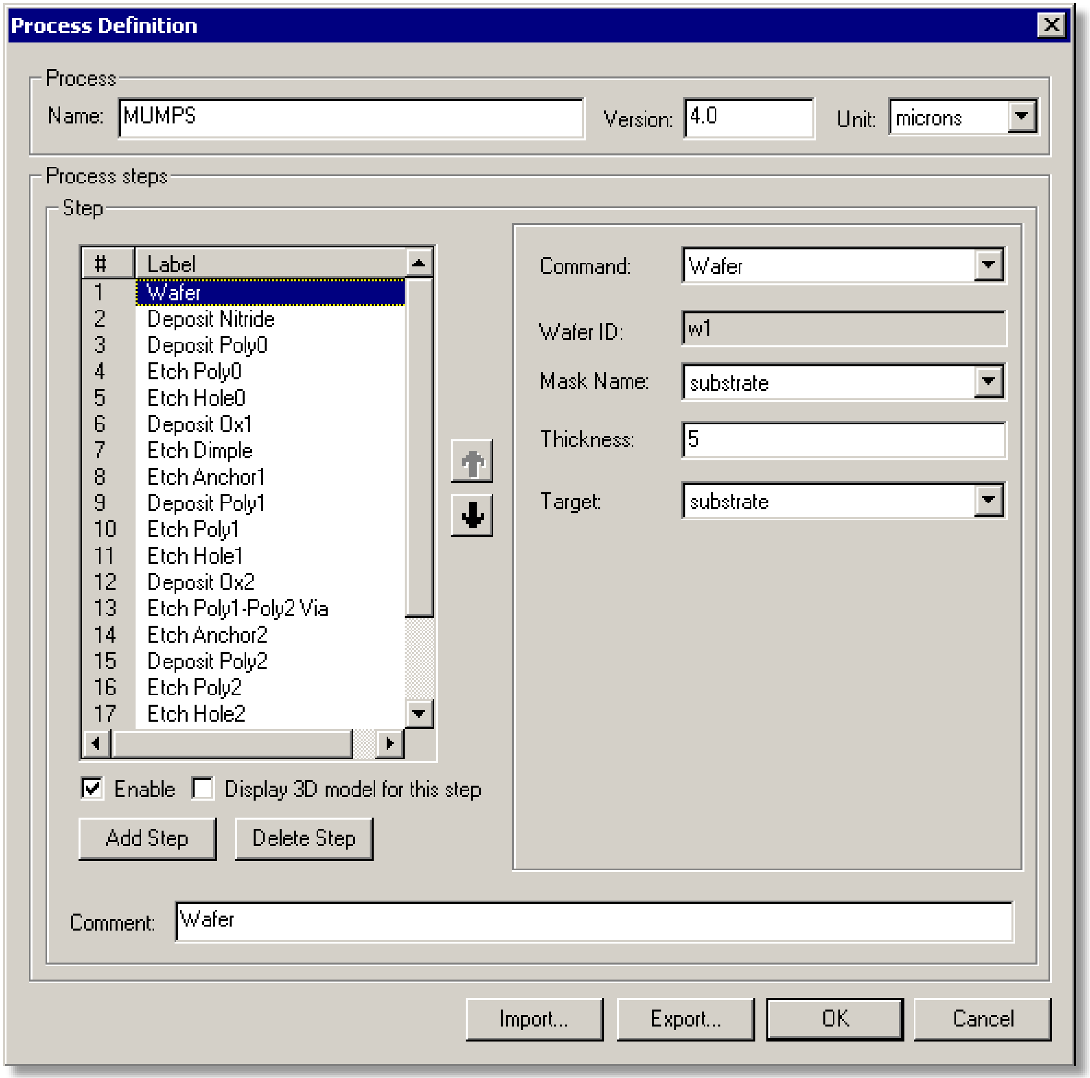
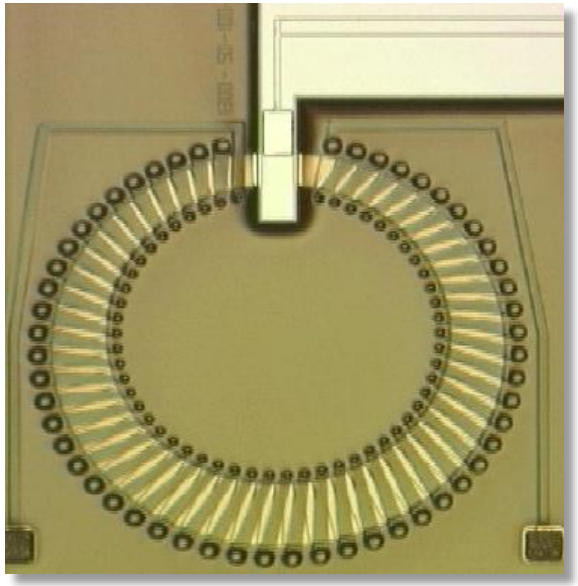
Fabrication Process Editor

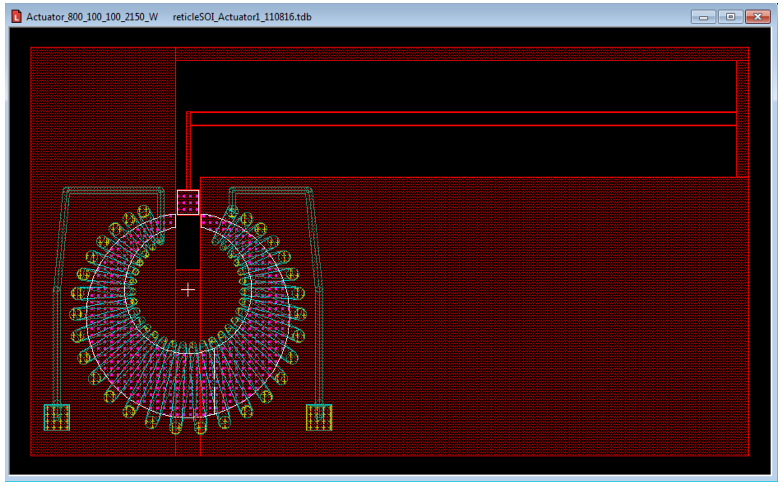
- Describes fabrication processing steps and sequence
- Commands:
  - Wafer manipulation
  - Deposit: Conformal, Snowfall, Fill
  - Etch: Isotropic, Aniostropic, Dry, etc
  - Implant
  - Grow
  - Mechanical Polish
  - Electroplating
  - Wafer Stacking



Mask/Process Co-design

- Designers and process engineers collaborate
- Process compatibility checked
- Find fabrication issues
- Communicate between fab & design house
- Predict shape, predict performance





Step

#	Label
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2	Permanent Magnet Deposit
3	DRIE Etch
4	Permanent Magnet Etch
5	DRIE Hard Mask Deposit
6	DRIE Hard Mask Etch
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8	Protection Metal Deposition
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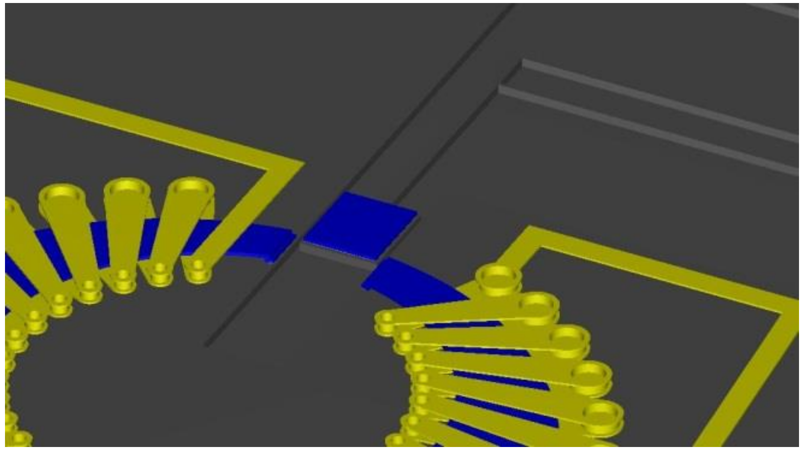
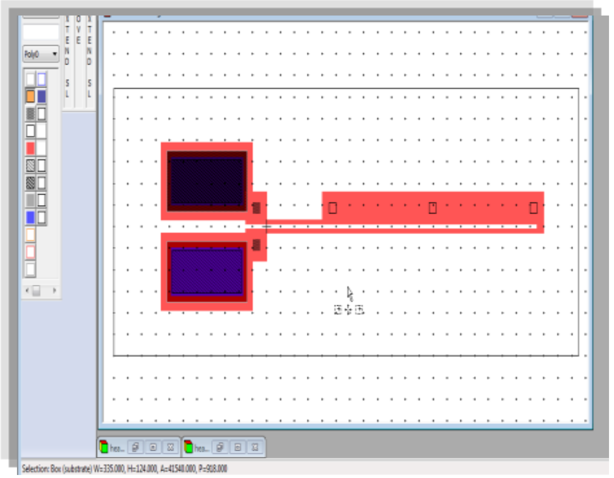
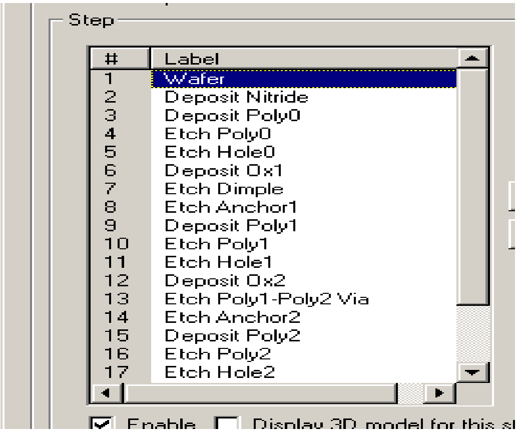
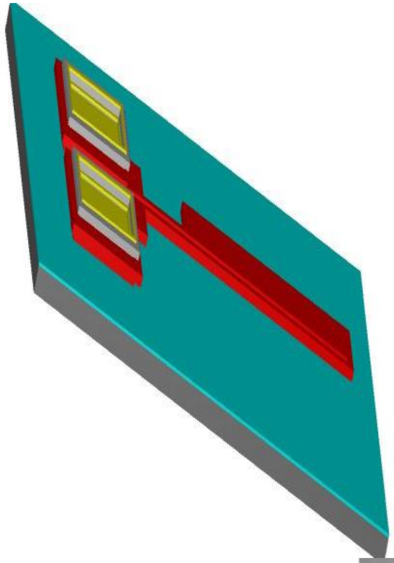


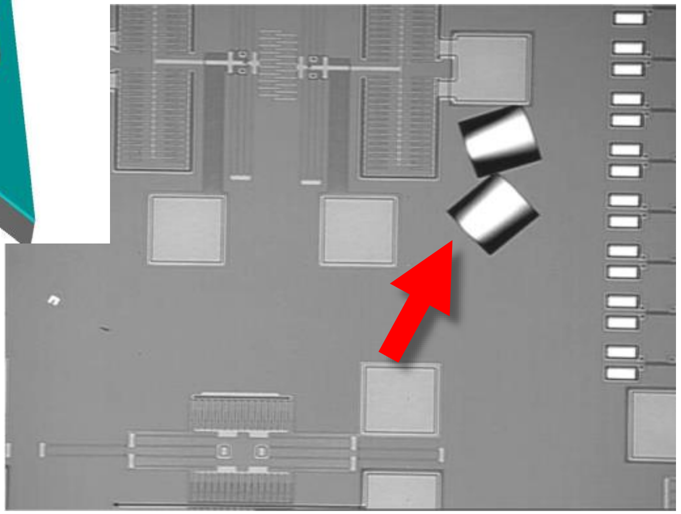
Virtual Prototyping

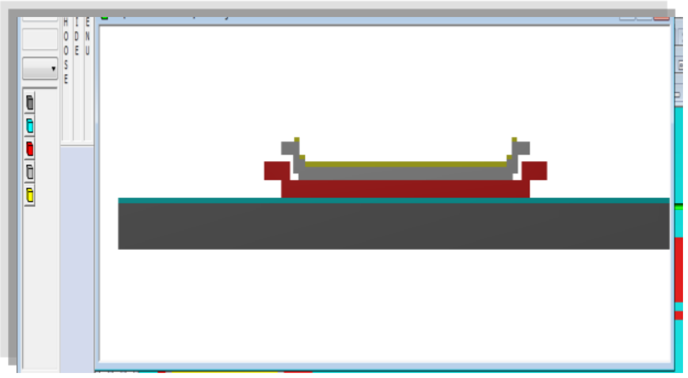
- New designers can learn
- Example: Improperly anchored Pad

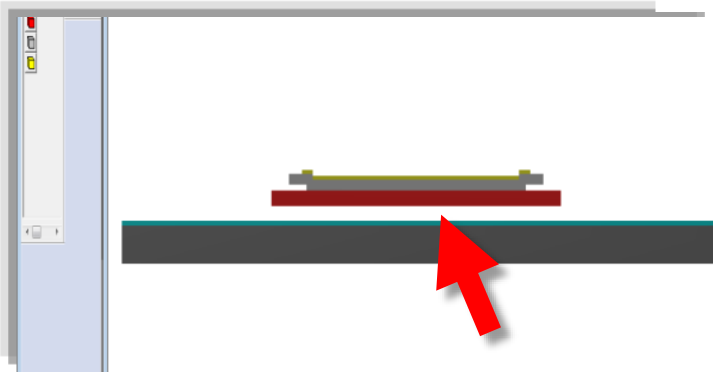










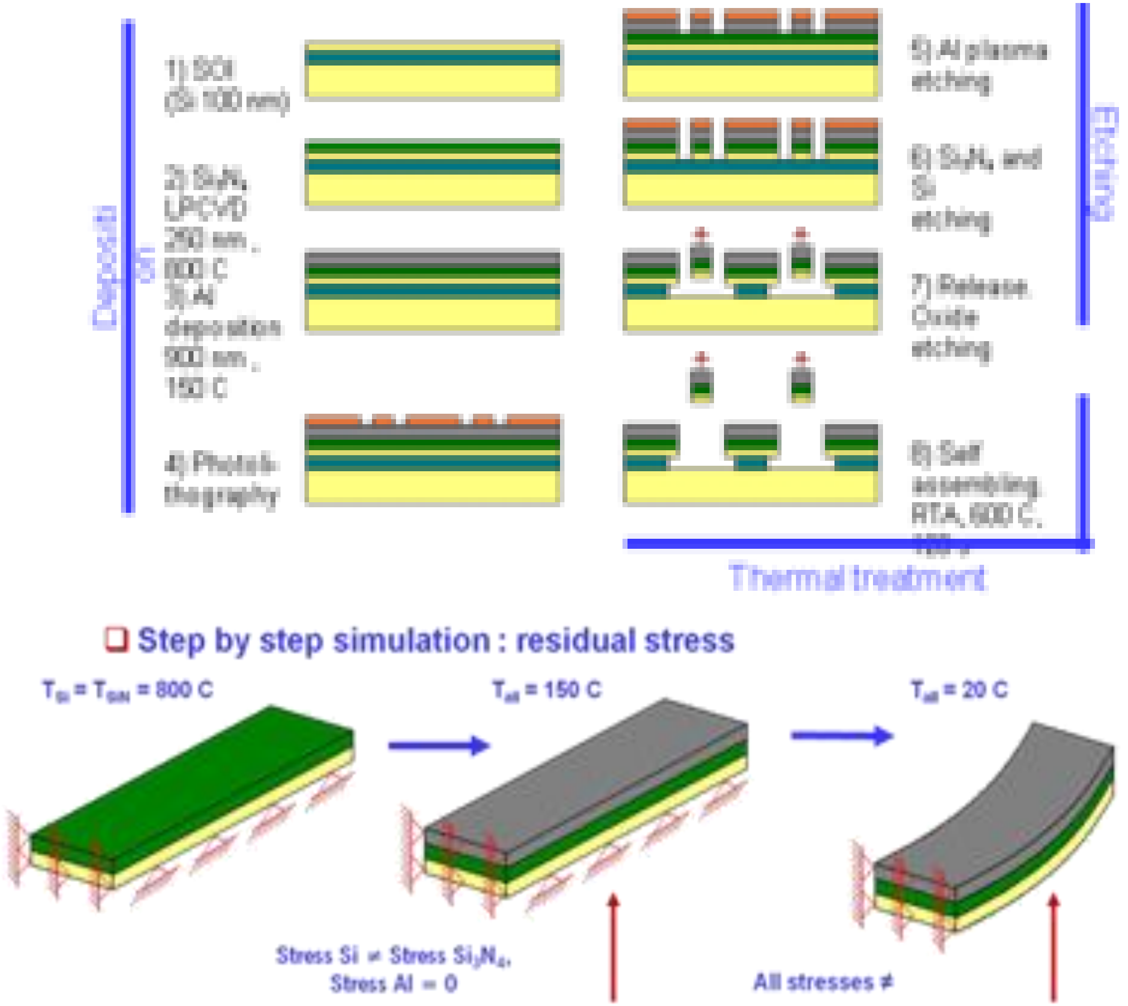


Source: Joel Kubby, UCSC

Material Properties

- Material properties depend on deposition conditions unique to fab process
- Pre-stress in materials effect performance
- Important to simulate using the correct material properties
- CAD can help to characterize materials

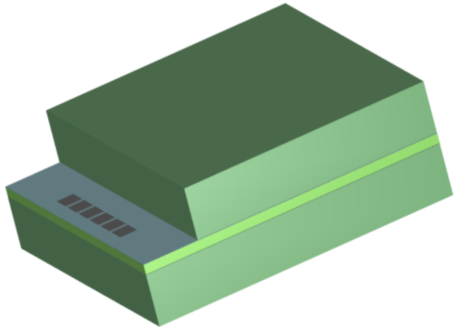
Full FAB-process Simulation

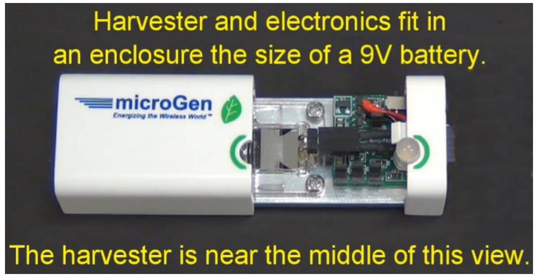


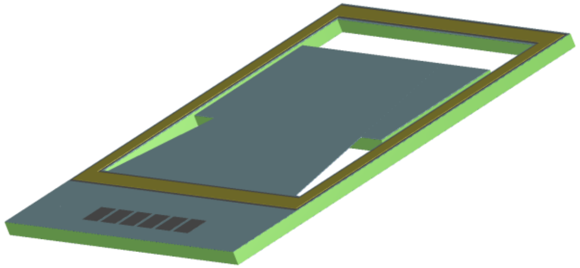
Package Modeling

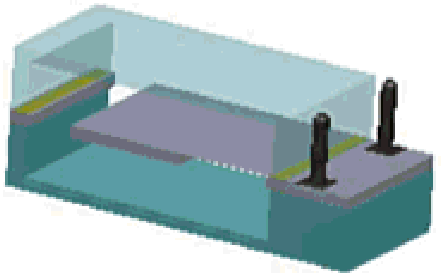
microGen
Energizing the Wireless World™

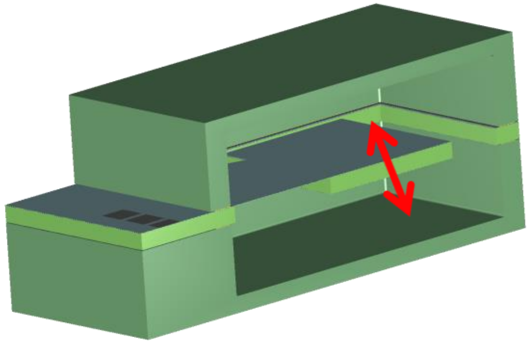
- MEMS package determines device performance
- Co-Design MEMS + Package
- Energy Harvester
  - Visual The Device
  - Communicate With The Fab
  - Create 3D Model of MEMS And Package For FEM Analysis
  - Virtual Prototyping
  - Coupled Fluid-Mechanical-Piezo-Electric Simulation

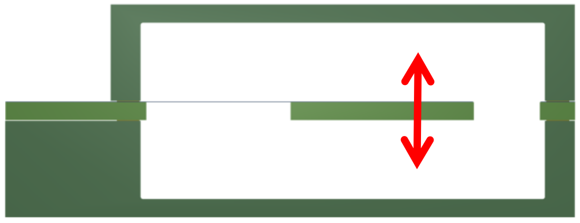












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MEMS Packaging – Mechanical Robustness

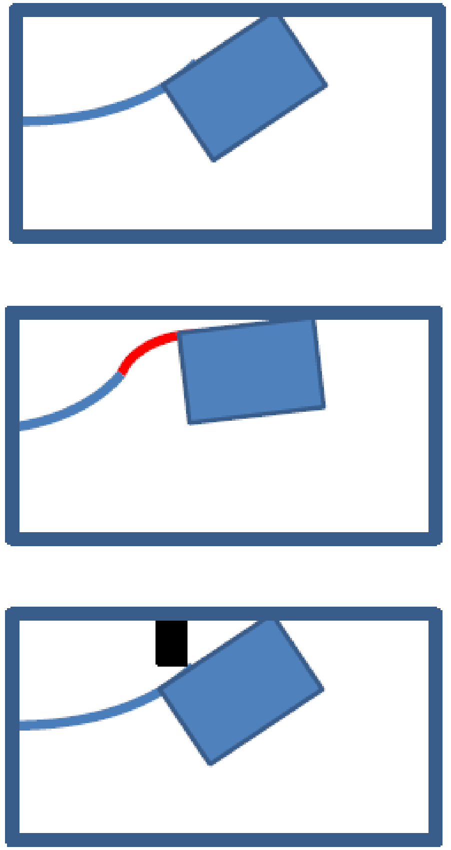
Impact "Stopper"

desired

What is happening

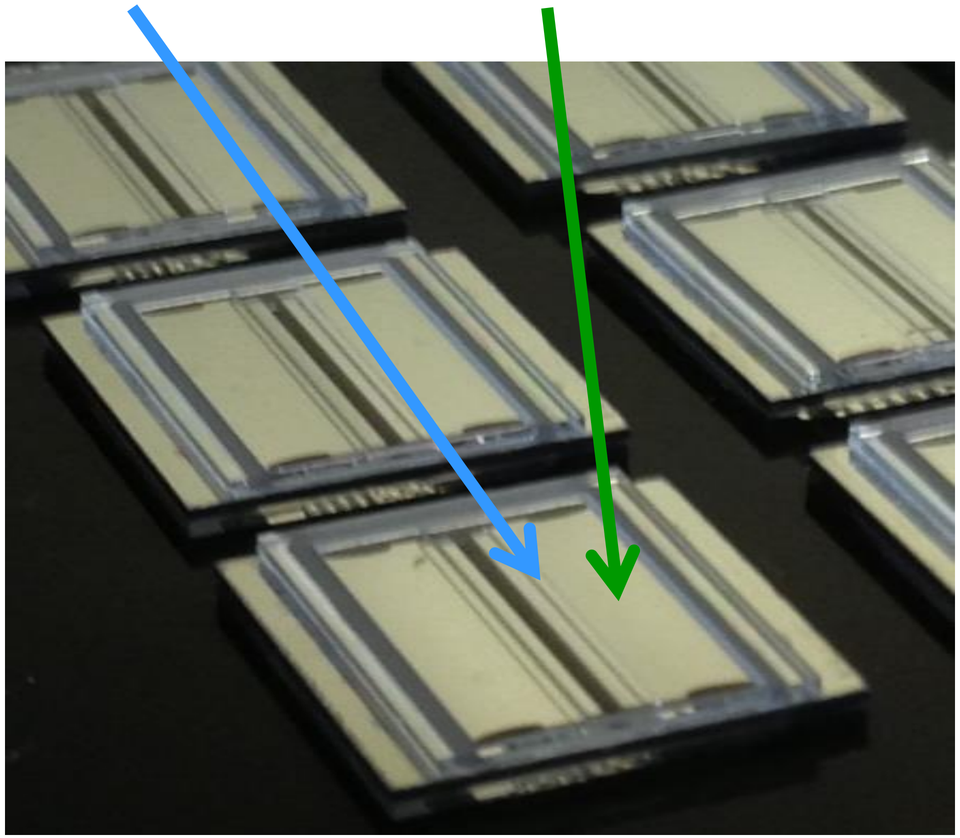
High strain causes fracture

Corrected with "stopper"



stopper

cantilever

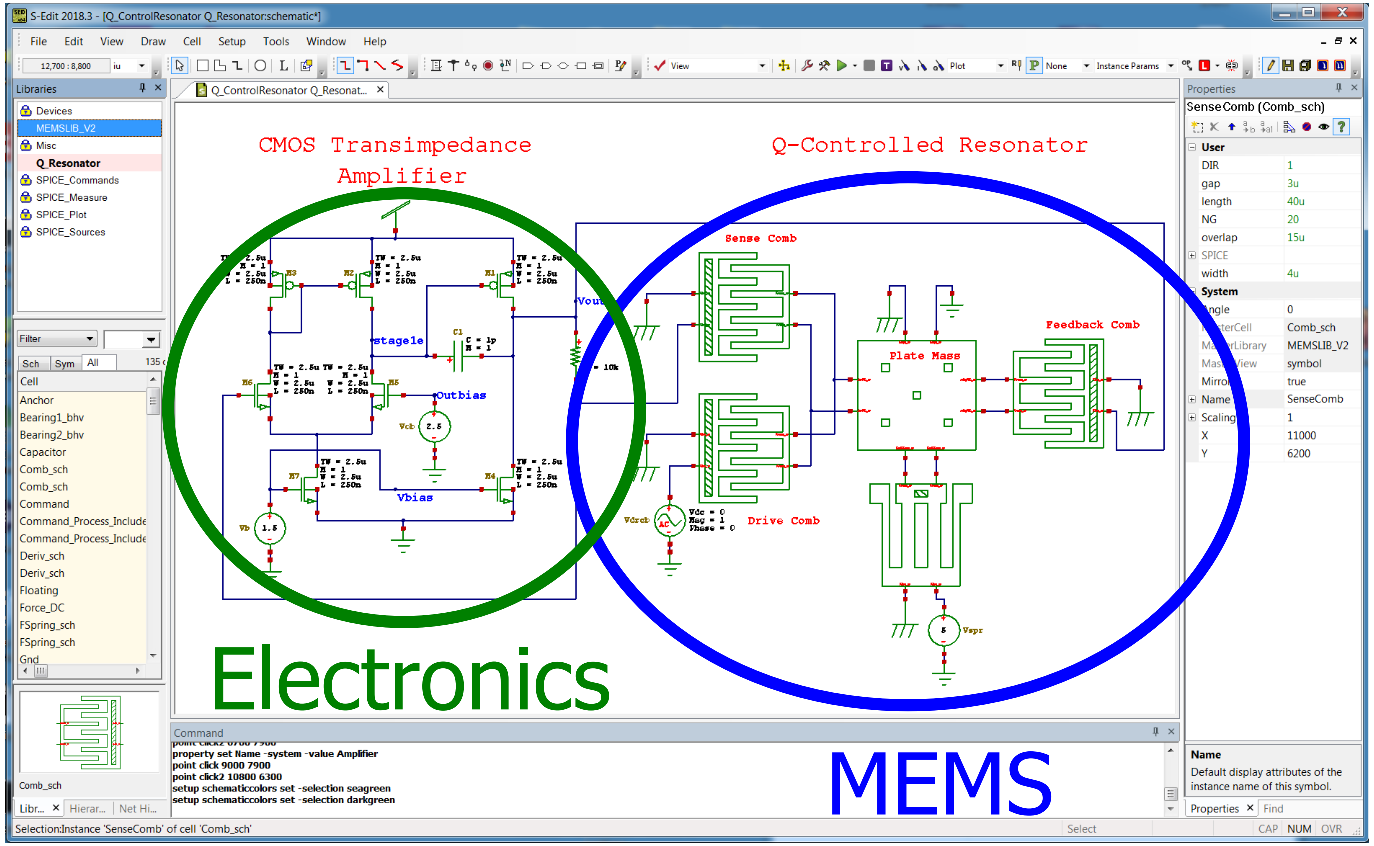


softMEMS *Source: MicroGen*

SYSTEM LEVEL SIMULATION

MEMS & IC Co-Simulation

- Schematics can contain both IC & MEMS Devices
- IC modeled using standard TSMC IC SPICE models
- MEMS modeled using behavioral descriptions with mechanical, electrostatic, magnetic, fluidic disciplines
- MEMS models
  - No universal primitives as in digital design
  - Primitives may exist in application areas – i.e. beam, gaps, plate



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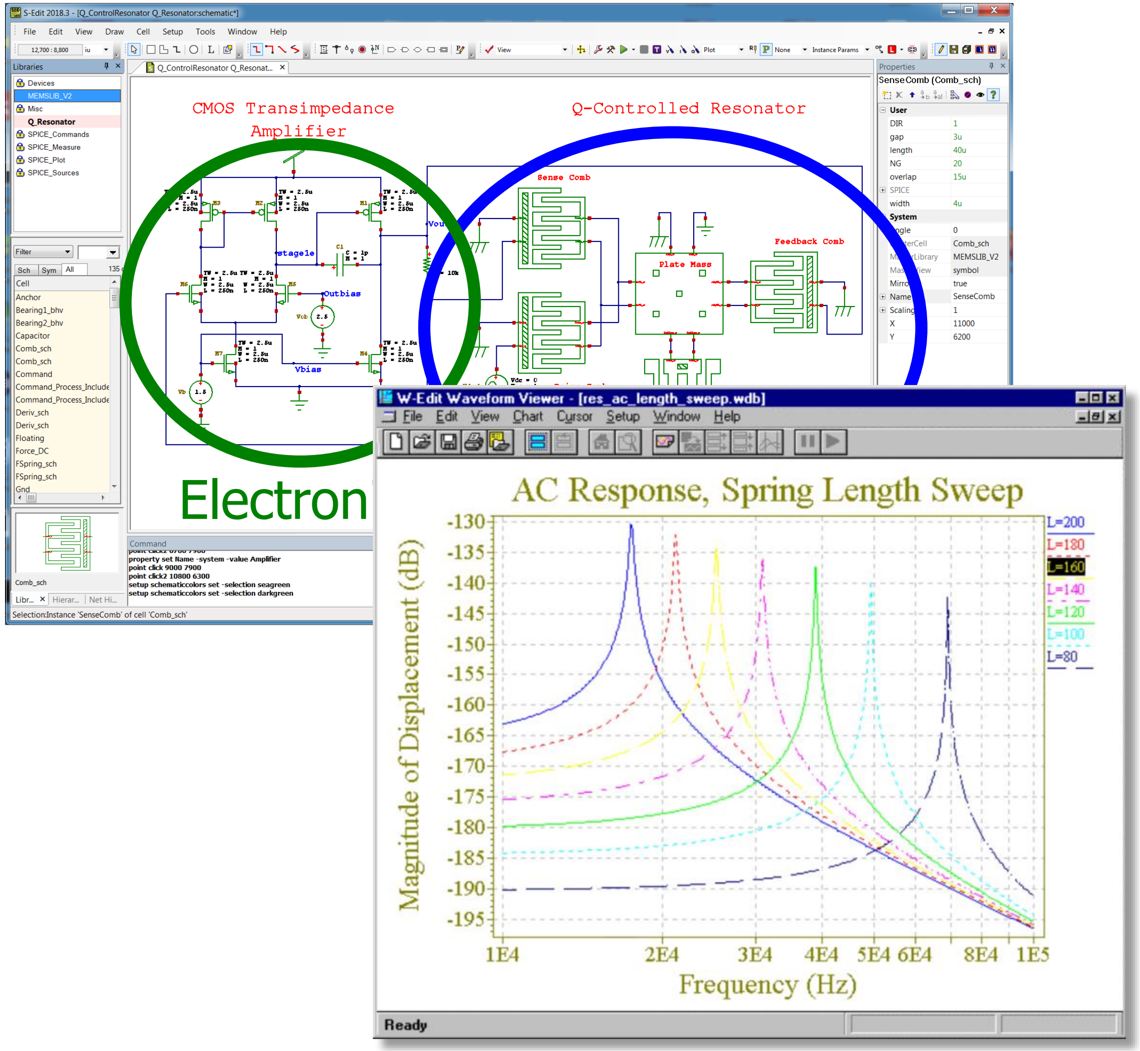
Approach to System Modeling

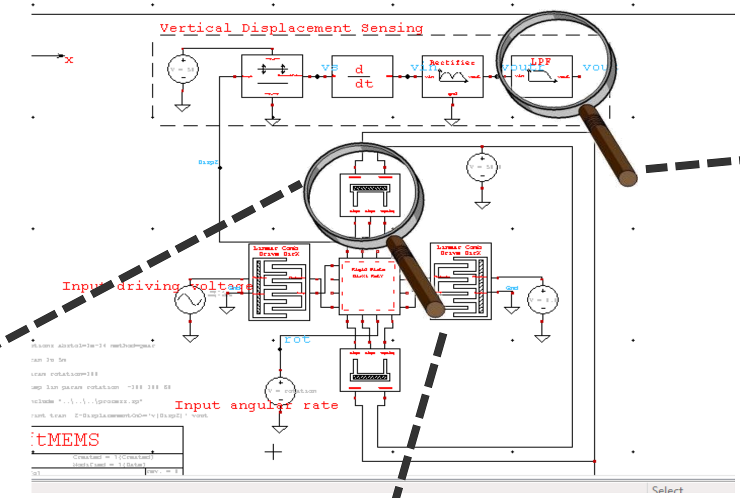
- Models can be used in T-Spice
  - — No universal primitives as in digital design
  - — Primitives may exist in application areas – i.e. beam, gaps, plate
- Create libraries of models when possible
- Supports Parametric, Transient, AC, and Noise Analysis
- Describe models with
  - — SPICE
  - — Verilog-A

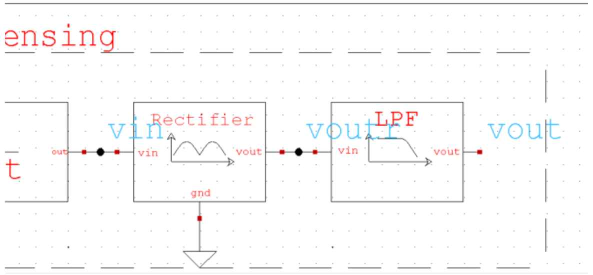


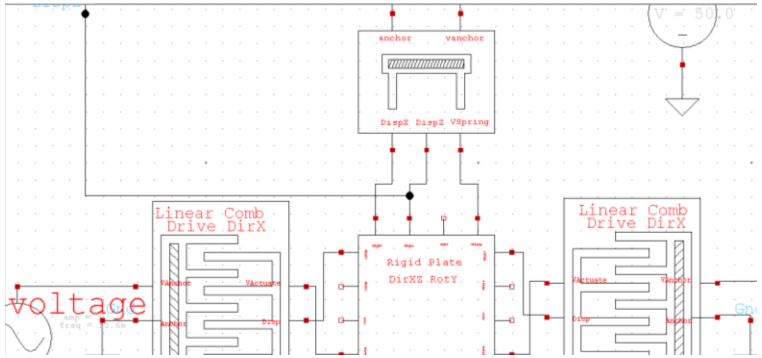
System Modeling- Circuits and Sensors

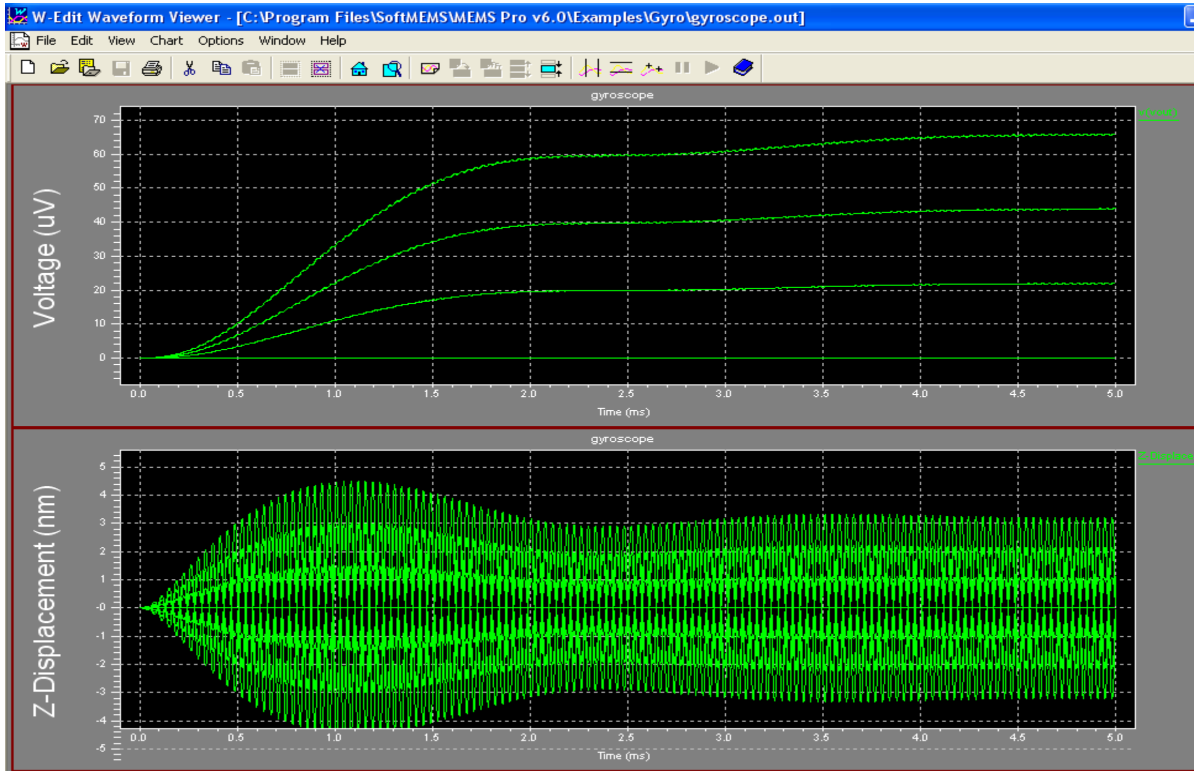
Input : AC voltage, Rotation

Gyroscope





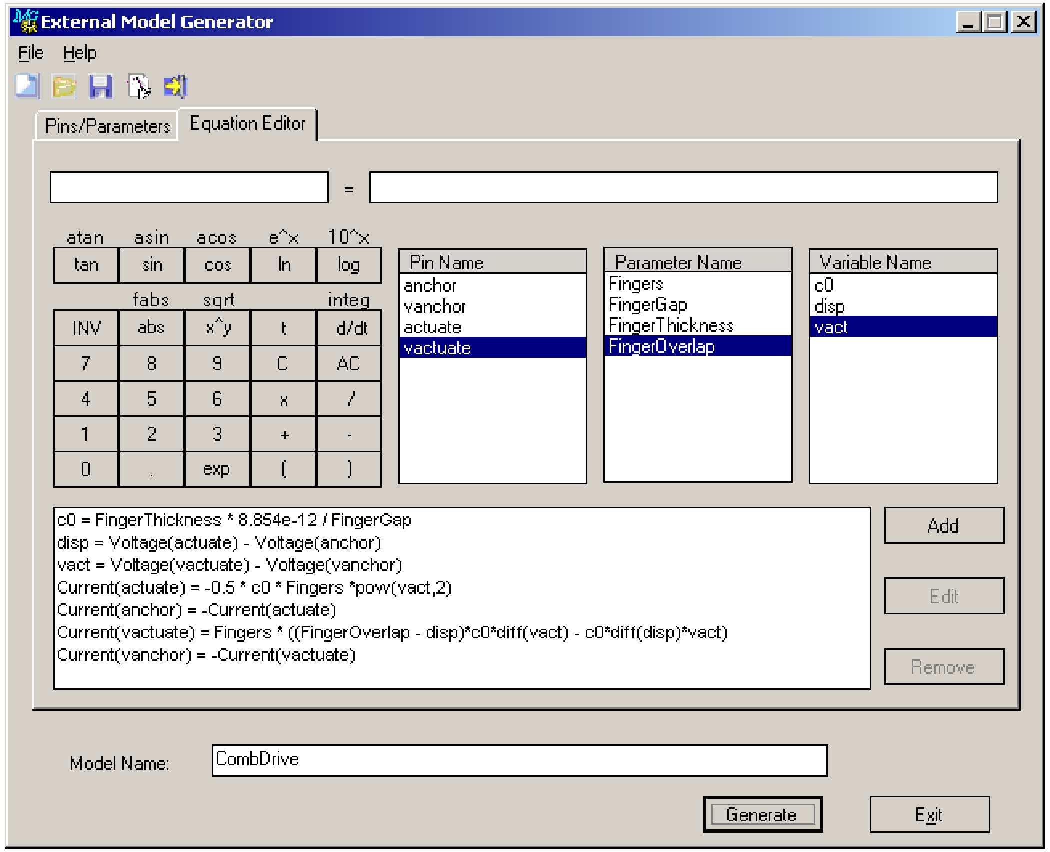


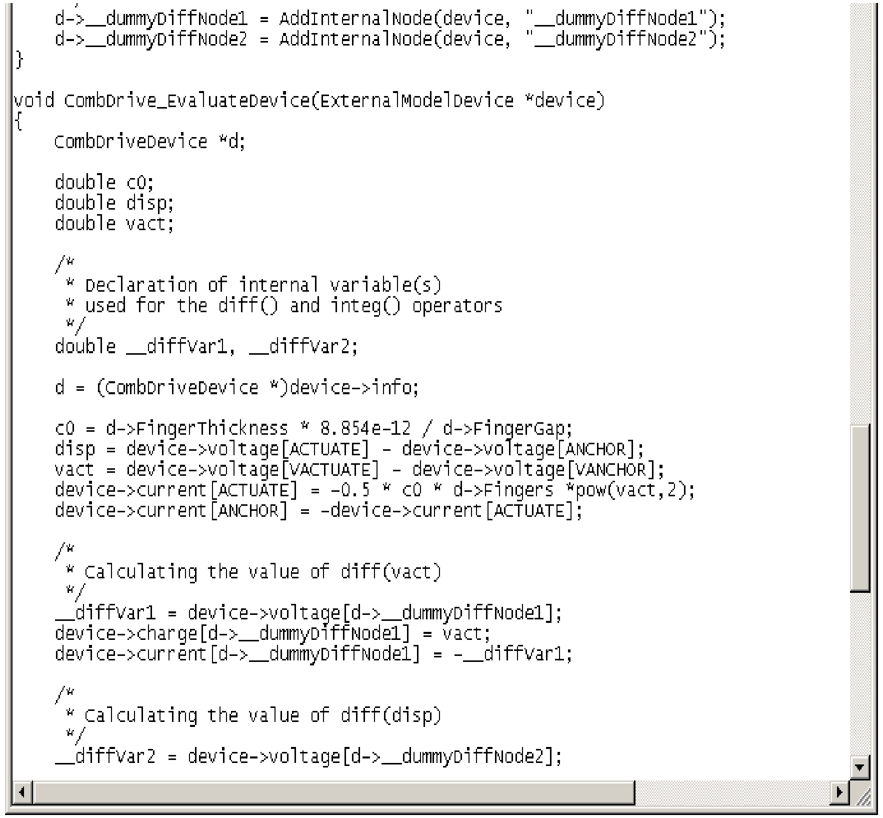


MODEL BUILDER

System Model Builder

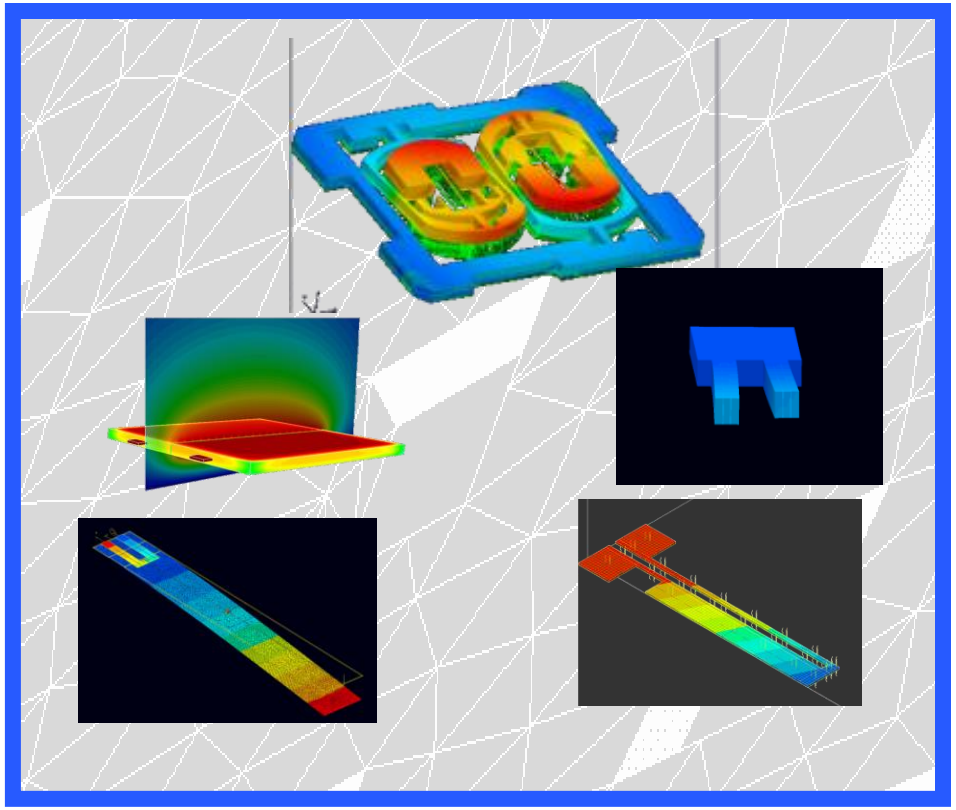
- Creates a model ready for simulation from analytical equations
- Outputs model in SPICE, C, Verilog-A, or VHDL-AMS



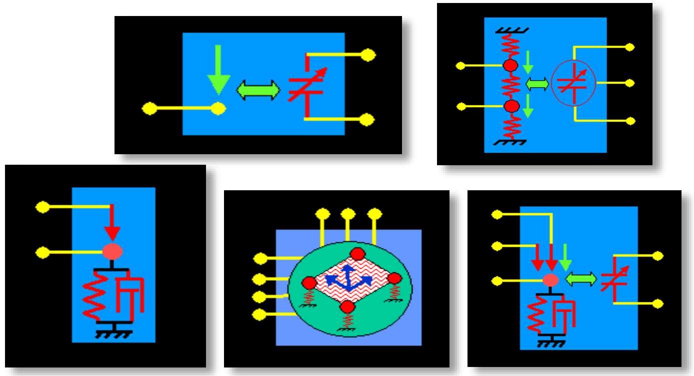


Compact Model Creation

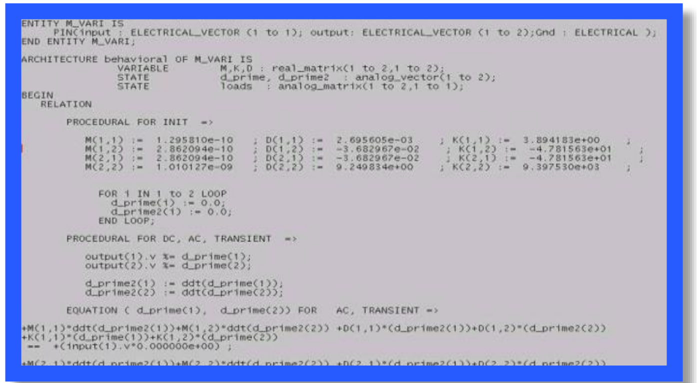
- MEMS must be analyzed in 3D
- Translate Results From A Coupled-Finite Element/Boundary Element Model Simulation To Behavioral Model



Compact Model Builder



SPICE



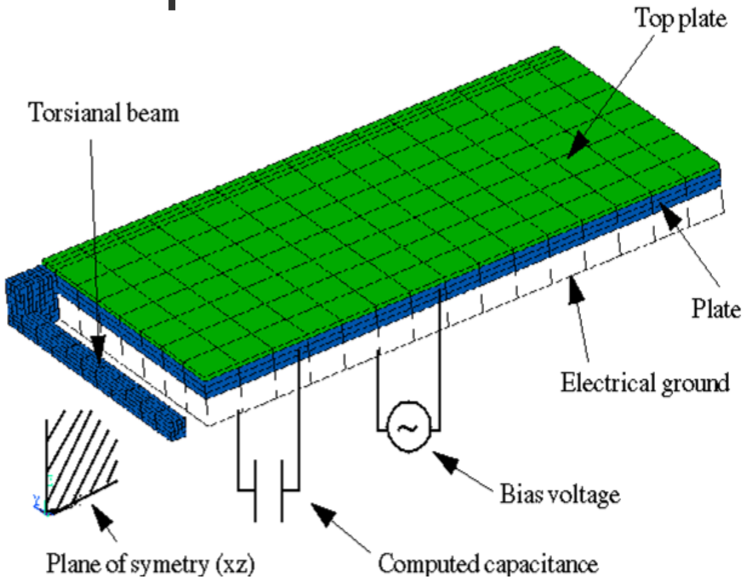
```
ENTITY M_VARI IS
    PIN(input : ELECTRICAL_VECTOR (1 to 1); output: ELECTRICAL_VECTOR (1 to 2);Gnd : ELECTRICAL );
END ENTITY M_VARI;

ARCHITECTURE behavioral OF M_VARI IS
          VARIABLE       M,K,D : real_matrix(1 to 2,1 to 2);
          STATE          d_prime, d_prime2  : analog_vector(1 to 2);
          STATE          loads   : analog_matrix(1 to 2,1 to 1);
BEGIN
  RELATION

     PROCEDURAL FOR INIT  =>

       M(1,1) :=  1.295810e-10   ; D(1,1) :=  2.695605e-03   ; K(1,1) :=  3.894183e+00   ;
       M(1,2) :=  2.862094e-10   ; D(1,2) :=  -3.682967e-02   ; K(1,2) :=  -4.781563e+01   ;
       M(2,1) :=  2.862094e-10   ; D(2,1) :=  -3.682967e-02   ; K(2,1) :=  -4.781563e+01   ;
       M(2,2) :=  1.010127e-09   ; D(2,2) :=  9.249834e+00   ; K(2,2) :=  9.397530e+03   ;

        FOR i IN 1 to 2 LOOP
          d_prime(i) := 0.0;
          d_prime2(i) := 0.0;
        END LOOP;

     PROCEDURAL FOR DC, AC, TRANSIENT  =>

       output(1).v %= d_prime(1);
       output(2).v %= d_prime(2);

       d_prime2(1) := ddt(d_prime(1));
       d_prime2(2) := ddt(d_prime(2));

     EQUATION ( d_prime(1),  d_prime(2)) FOR   AC, TRANSIENT =>

+M(1,1)*ddt(d_prime2(1))+M(1,2)*ddt(d_prime2(2)) +D(1,1)*(d_prime2(1))+D(1,2)*(d_prime2(2))
+K(1,1)*(d_prime(1))+K(1,2)*(d_prime(2))
 ==  +(input(1).v*0.000000e+00) ;
```

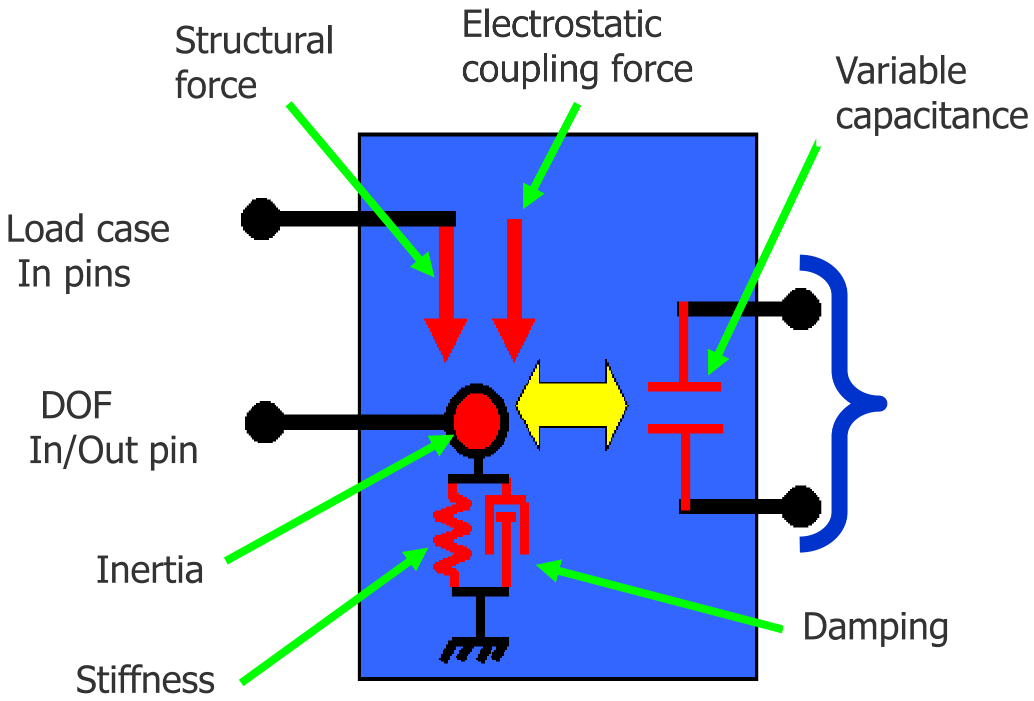
Verilog-A

Source: Open Engineering

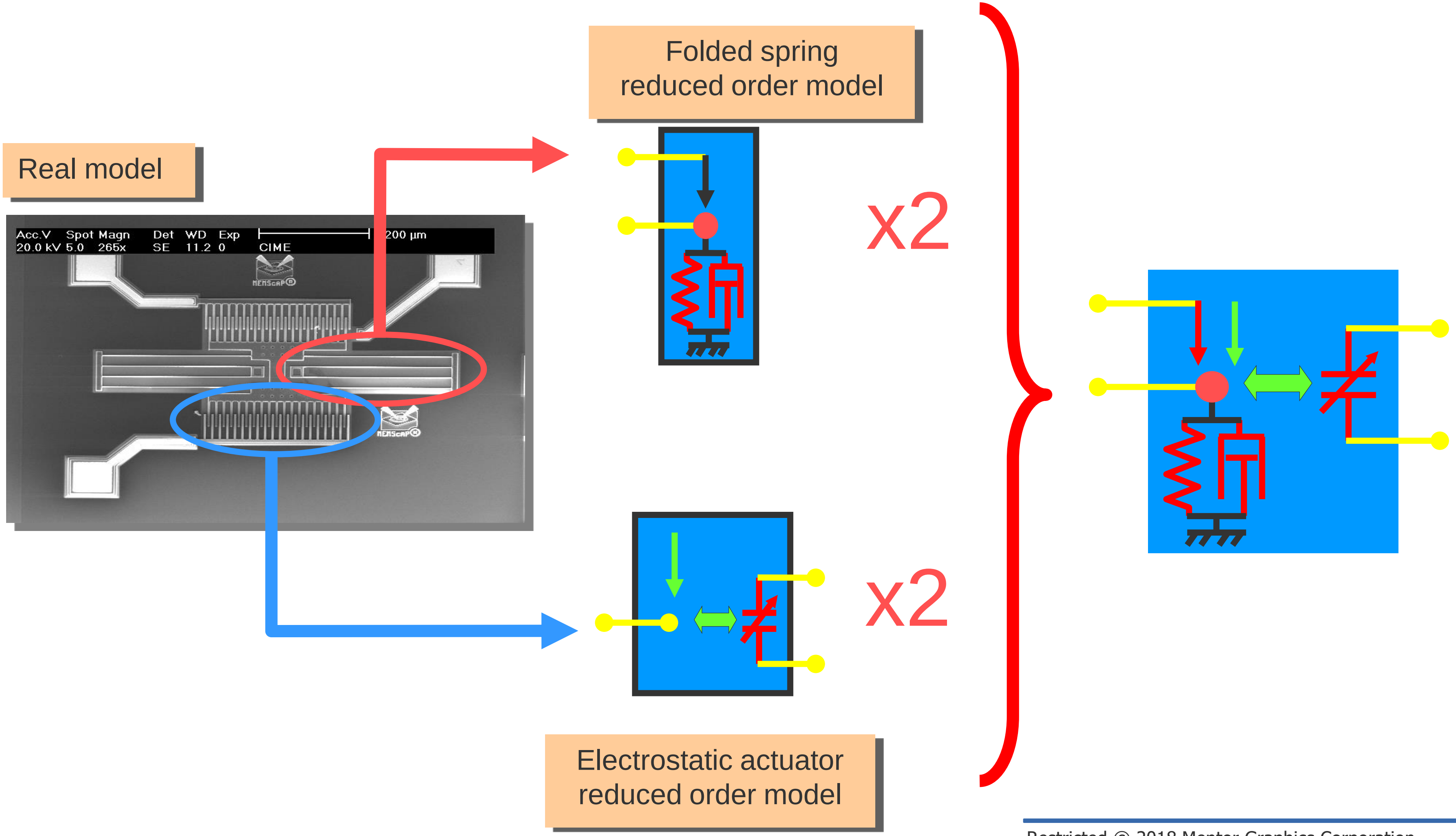
Compact Model Builder

- Reduced Order Model Generation From FEM Results
- Handles Coupled Electrostatic-Structural Reduction
- Handles Multiple Degrees Of Freedoms
- Linear Combination of Models
- Pull-In Voltage Computation
- Fluid Structure





Compact Model Builder-Assembly



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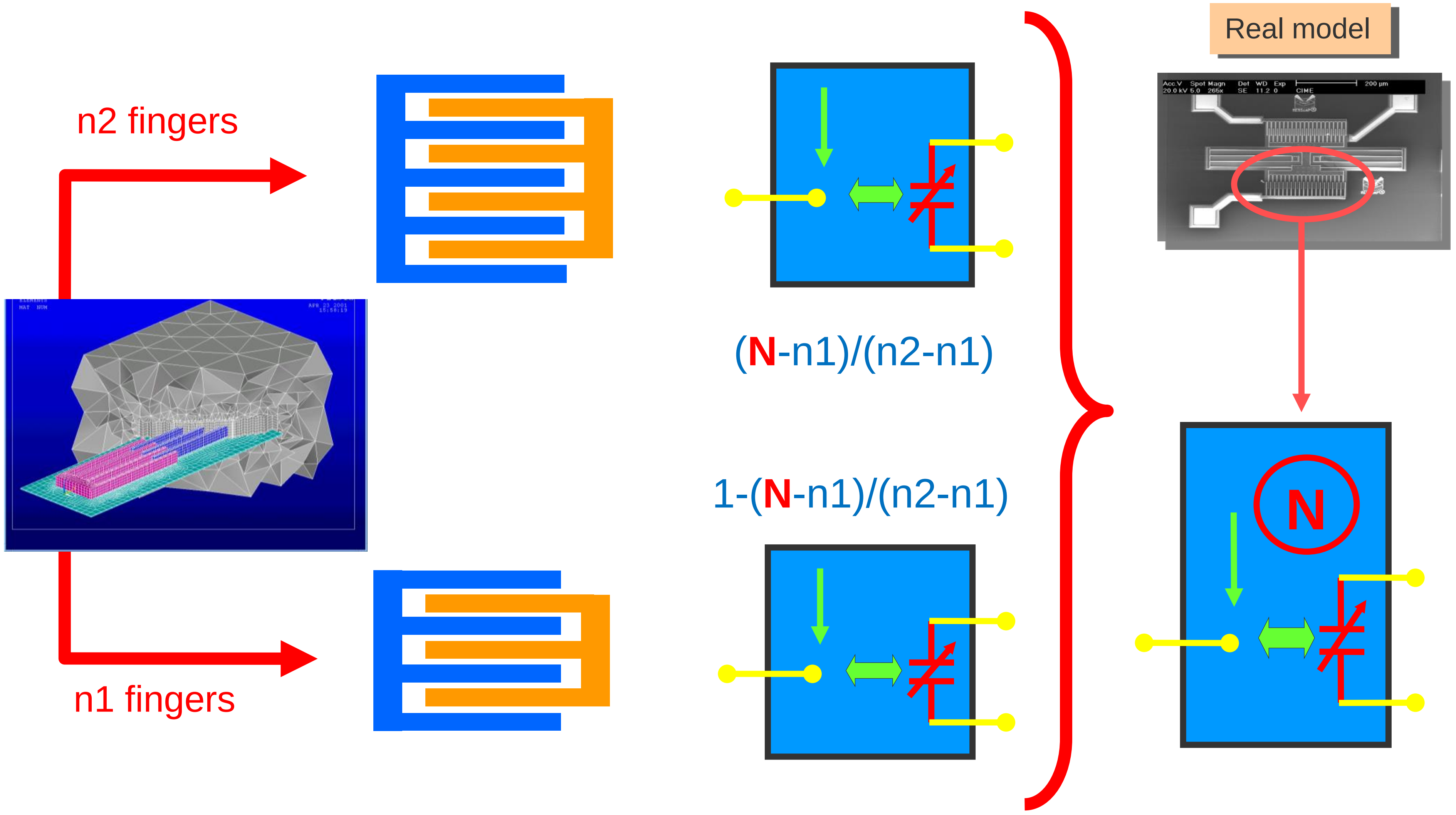
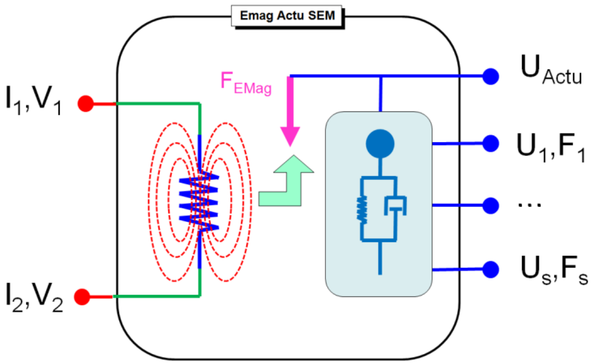
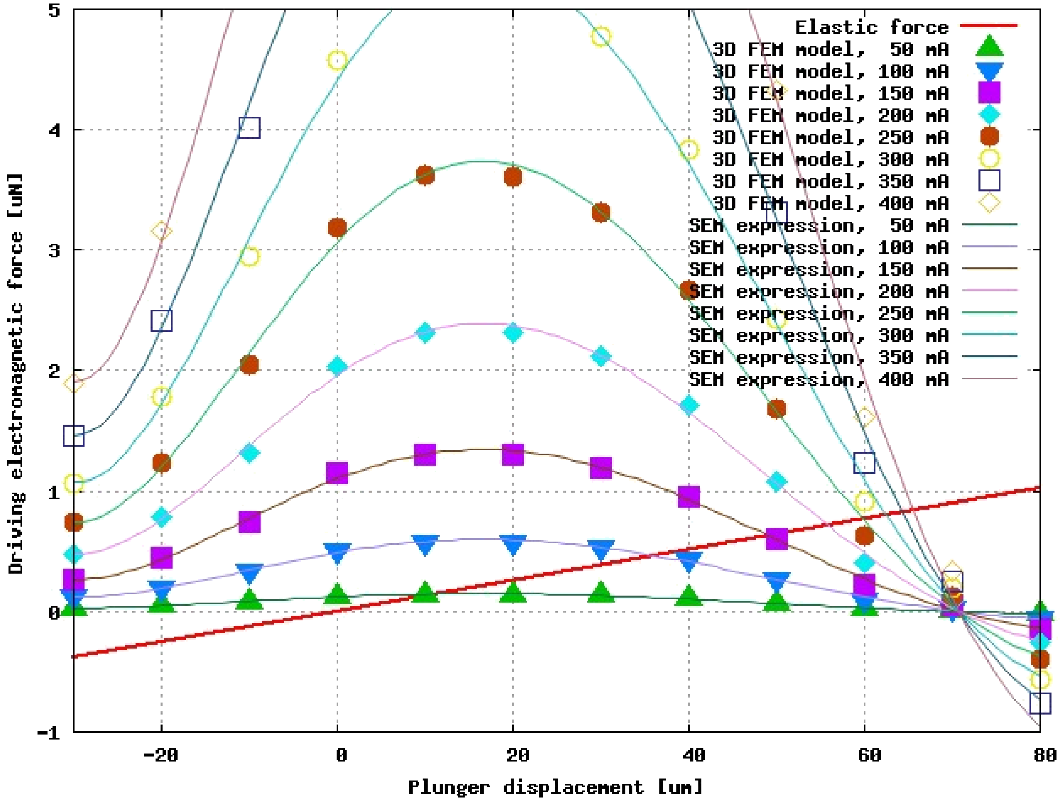
Compact Model Builder-Parametric models



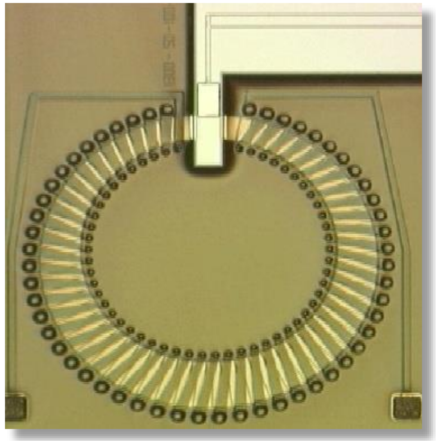
Example-Coupled Magnetic-Mechanical MEMS

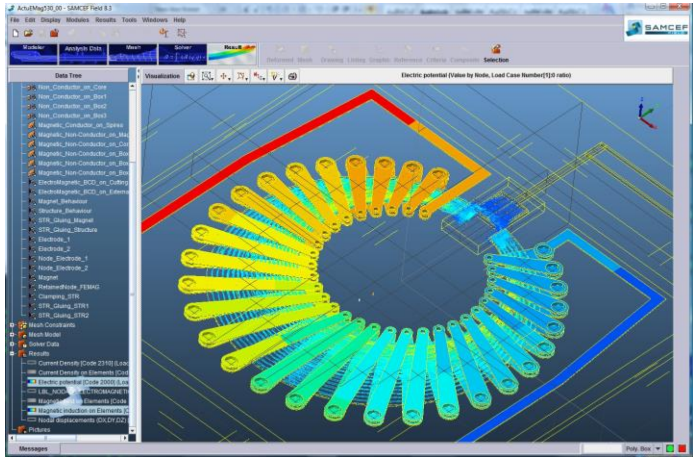
- Magnetic Actuator
- Couple magnetics to mechanics
- Enable system simulation
- System design trade-offs





Source: Advanced Micro sensors

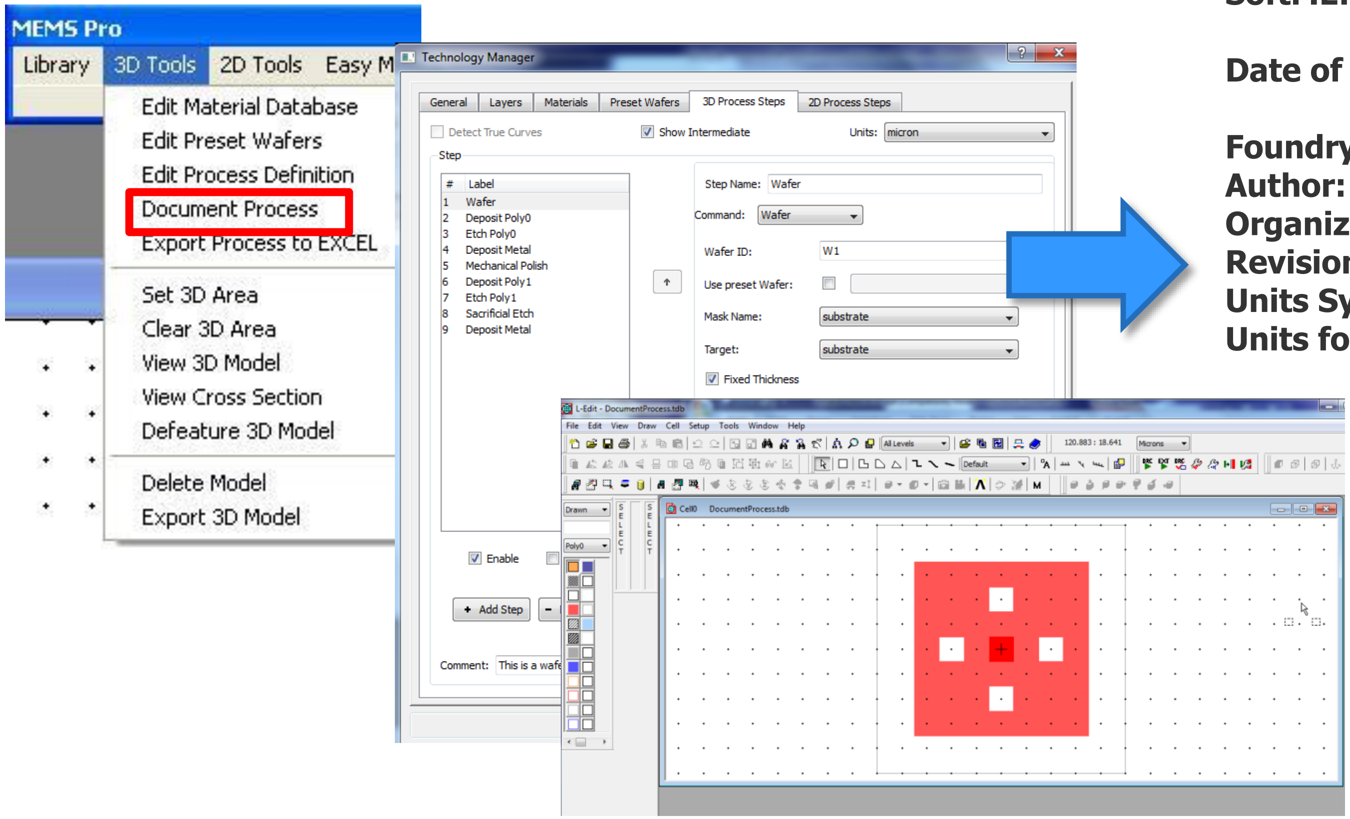




DESIGN KITS FOR MEMS

Document Fabrication Process

- Creates HTML document from Process Description showing materials used and a cross-section of each fabrication step

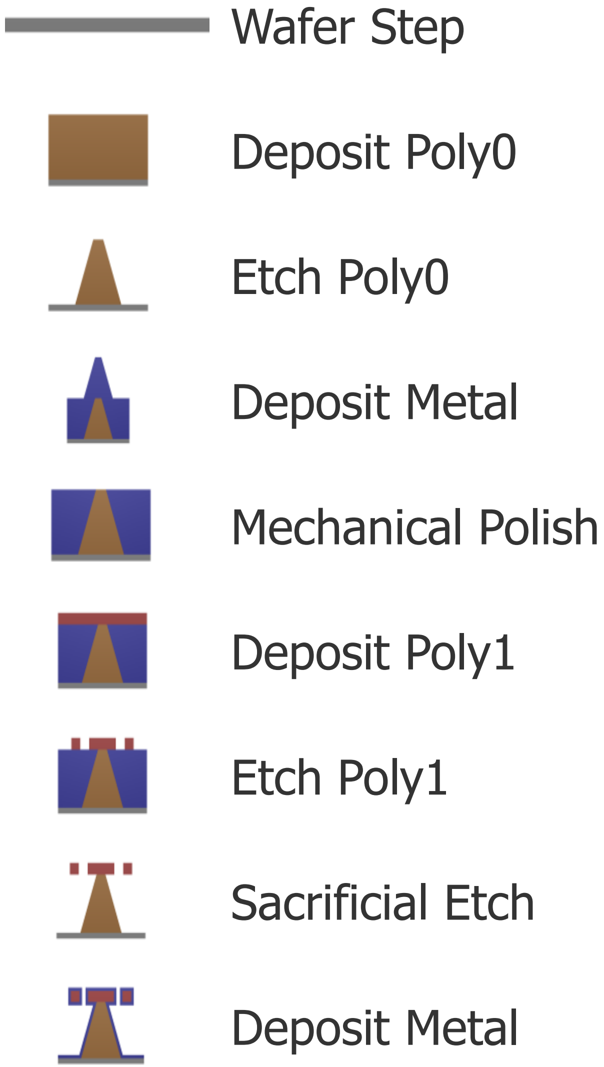


Process Documentation for: PolyMUMPs : SoftMEMS

Date of generation: 03/23/17 16:53:32

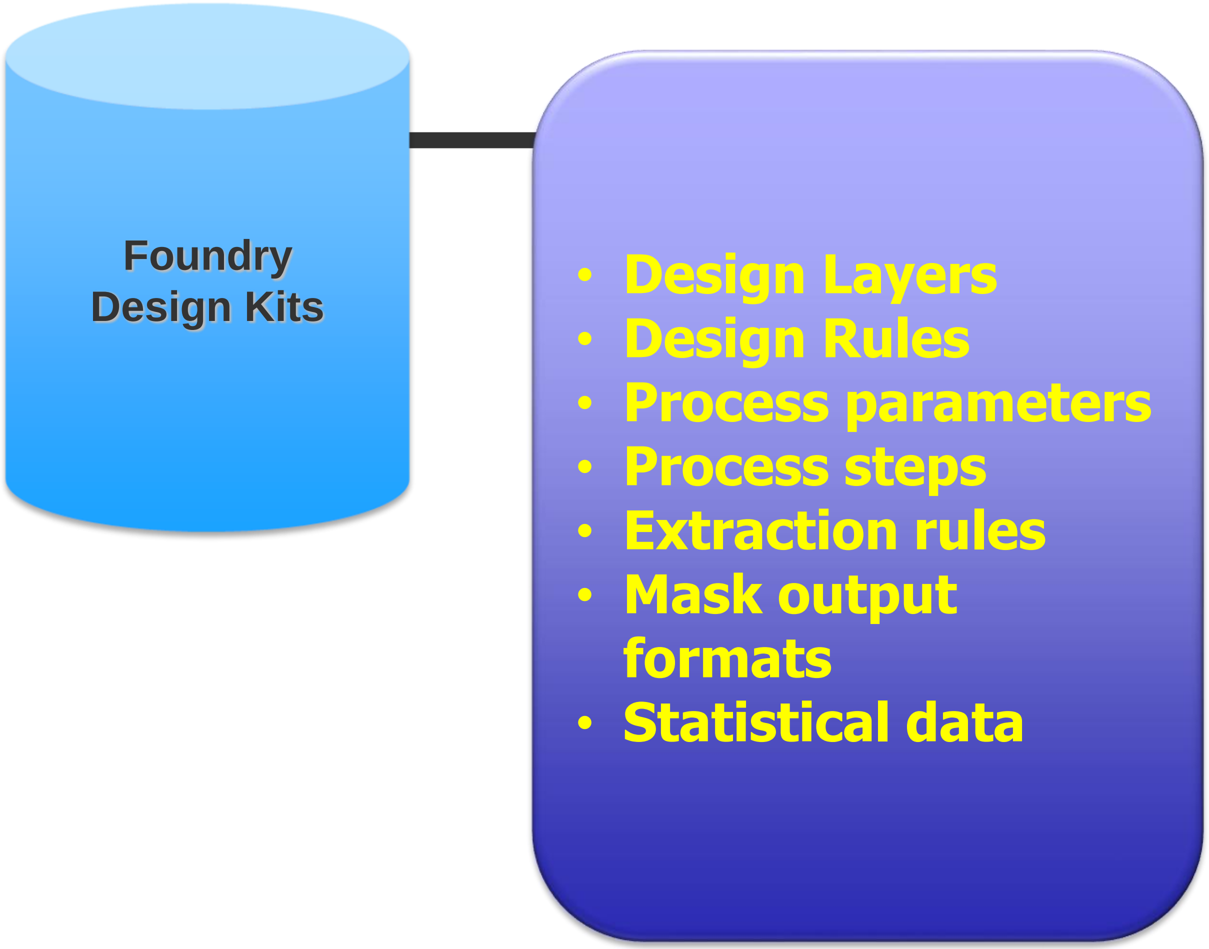
Foundry: SoftMEMS
Author: SoftMEMS
Organization: SoftMEMS
Revision No: 1.00
Units System: SI
Units for steps: micron

Materials List
Substrate
Poly0
Metal
Poly1



Design Kits

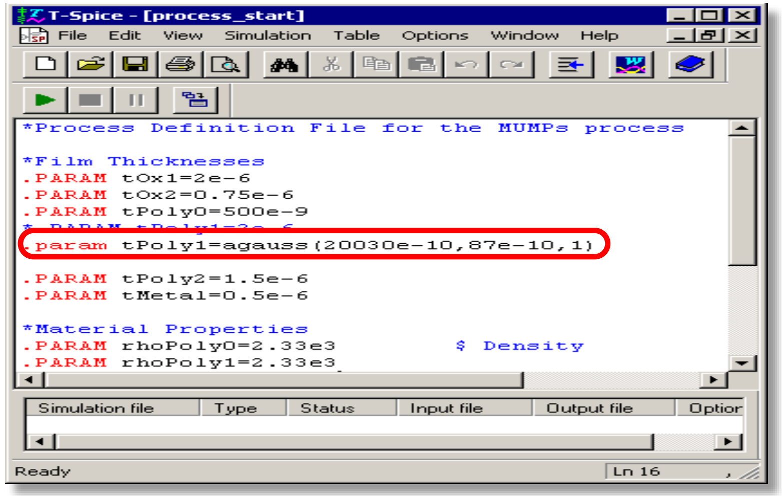
- Standardize information exchange, even if not for standard process
- Modeling formats, material properties, design rules
- Tech Transfer success - the more that is documented the higher success rate

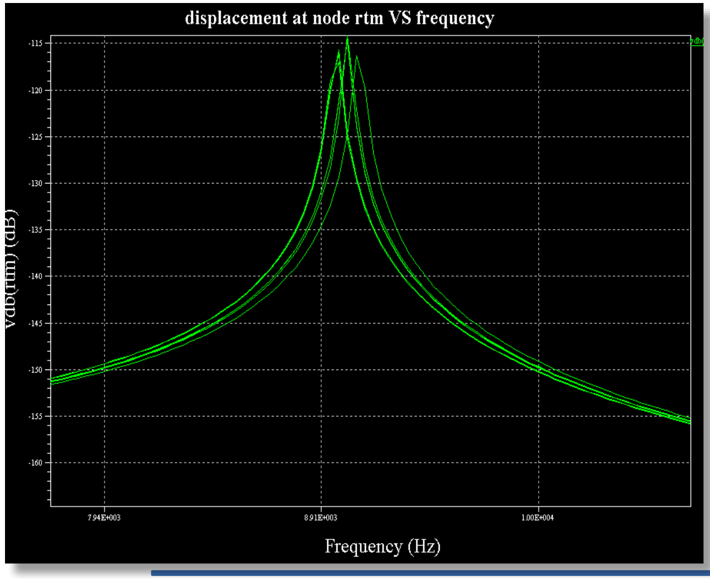


DESIGN FOR MANUFACTURABILITY FOR MEMS

Statistical Analysis

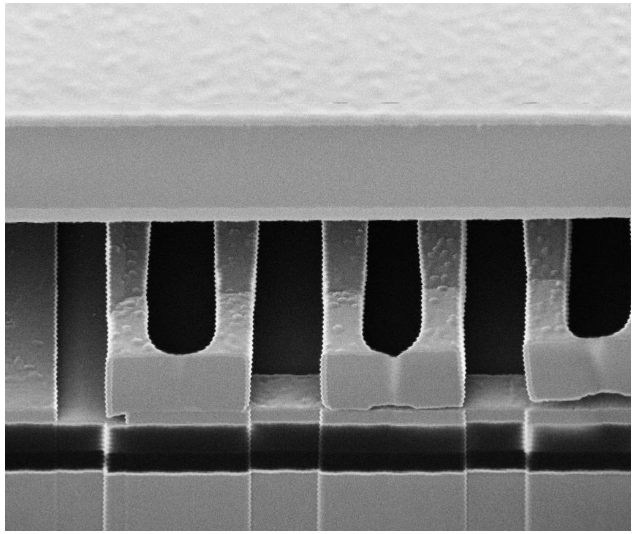
- Statistical analysis based on process/mask variations
  - Incorporates statistical data from foundries
  - Monte Carlo, Yield analyses
- Enables users to:
  - Develop process corners for simulation
  - Design centering
  - Calculate sensitivity

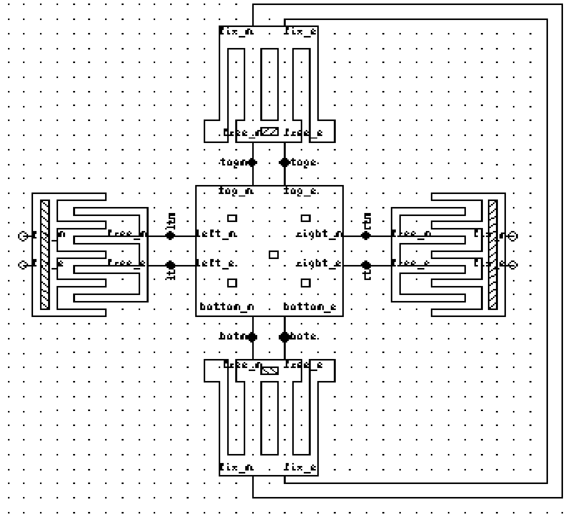


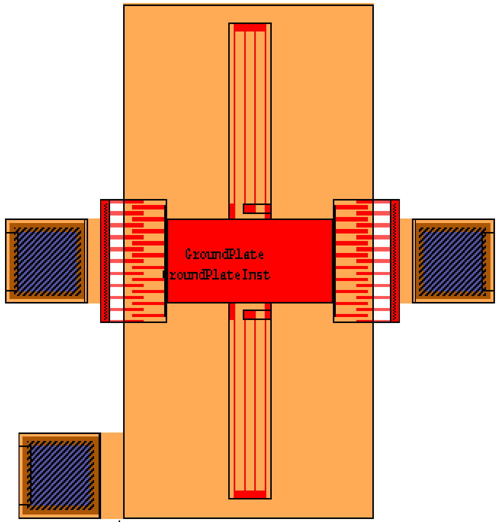


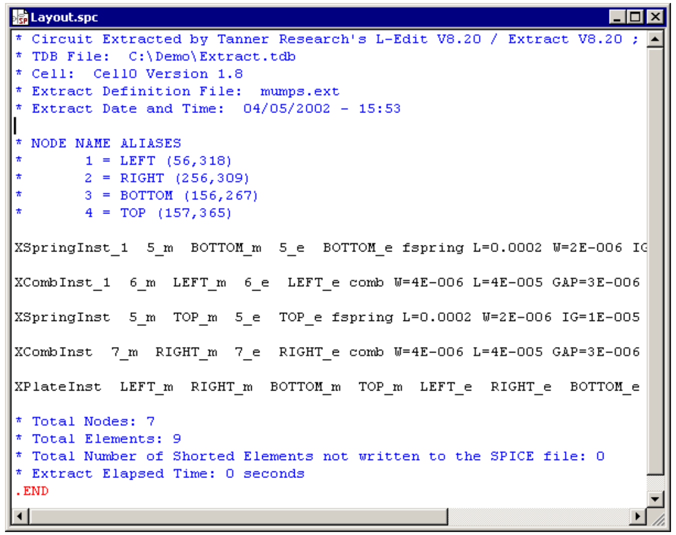
Parasitic Extraction and LVS

- MEMS devices must be simulated with their environment
- Problems occur if details left out
- Parasitics in multiple energy domains: thermal, electronic etc.
- Re-simulate after extraction of parasitics
- Create “multi-physics” netlist with parasitics included



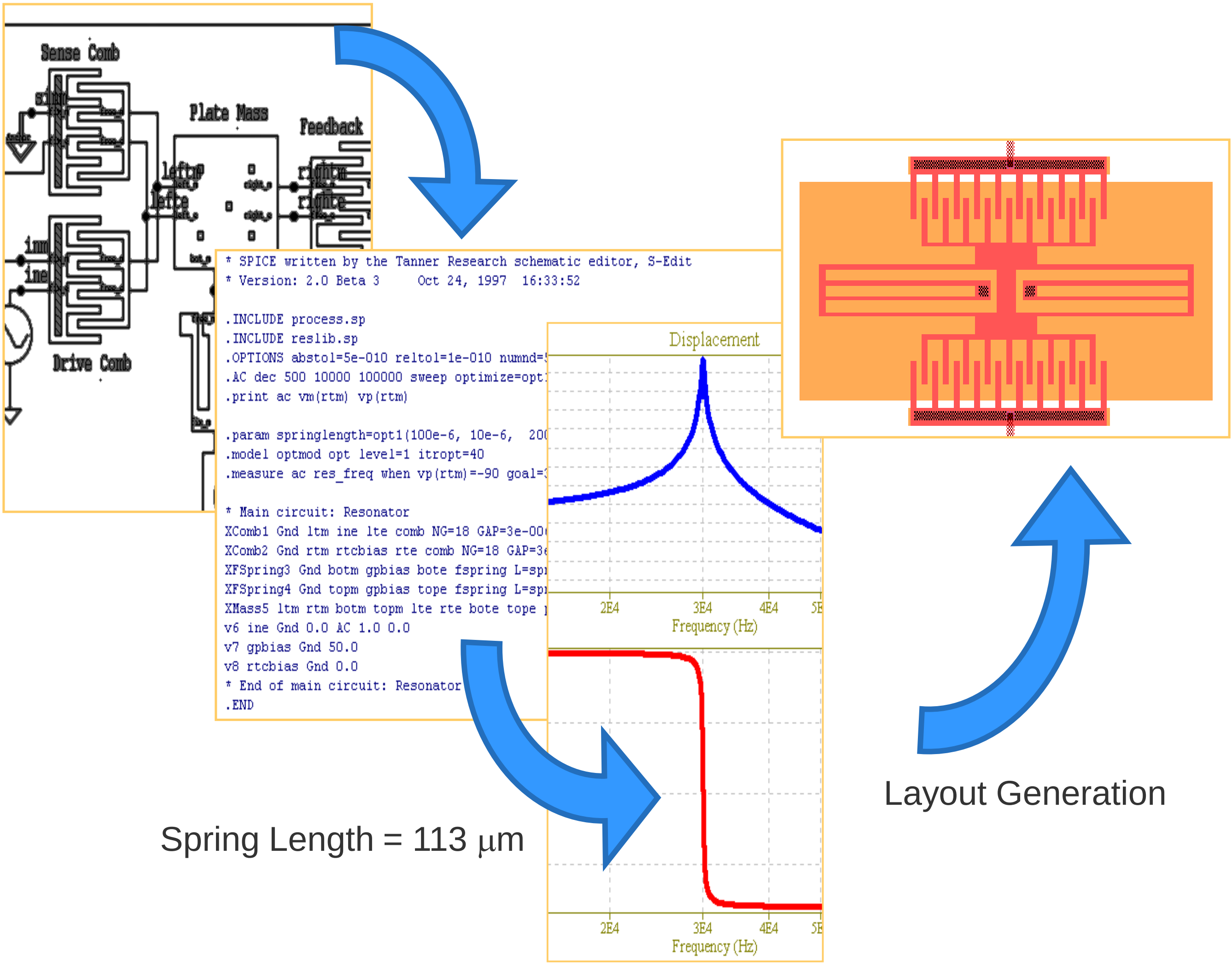





```
Layout.spc
* Circuit Extracted by Tanner Research's L-Edit V8.20 / Extract V8.20 ;
* TDB File:  C:\Demo\Extract.tdb
* Cell:  Cell0 Version 1.8
* Extract Definition File:  mumps.ext
* Extract Date and Time:  04/05/2002 - 15:53

* NODE NAME ALIASES
*       1 = LEFT (56,318)
*       2 = RIGHT (256,309)
*       3 = BOTTOM (156,267)
*       4 = TOP (157,365)

XSpringInst_1  5_m  BOTTOM_m  5_e  BOTTOM_e fspring L=0.0002 W=2E-006 IG

XCombInst_1  6_m  LEFT_m  6_e  LEFT_e comb W=4E-006 L=4E-005 GAP=3E-006

XSpringInst  5_m  TOP_m  5_e  TOP_e fspring L=0.0002 W=2E-006 IG=1E-005

XCombInst  7_m  RIGHT_m  7_e  RIGHT_e comb W=4E-006 L=4E-005 GAP=3E-006

XPlateInst  LEFT_m  RIGHT_m  BOTTOM_m  TOP_m  LEFT_e  RIGHT_e  BOTTOM_e

* Total Nodes: 7
* Total Elements: 9
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds
.END
```

Design for Manufacturing

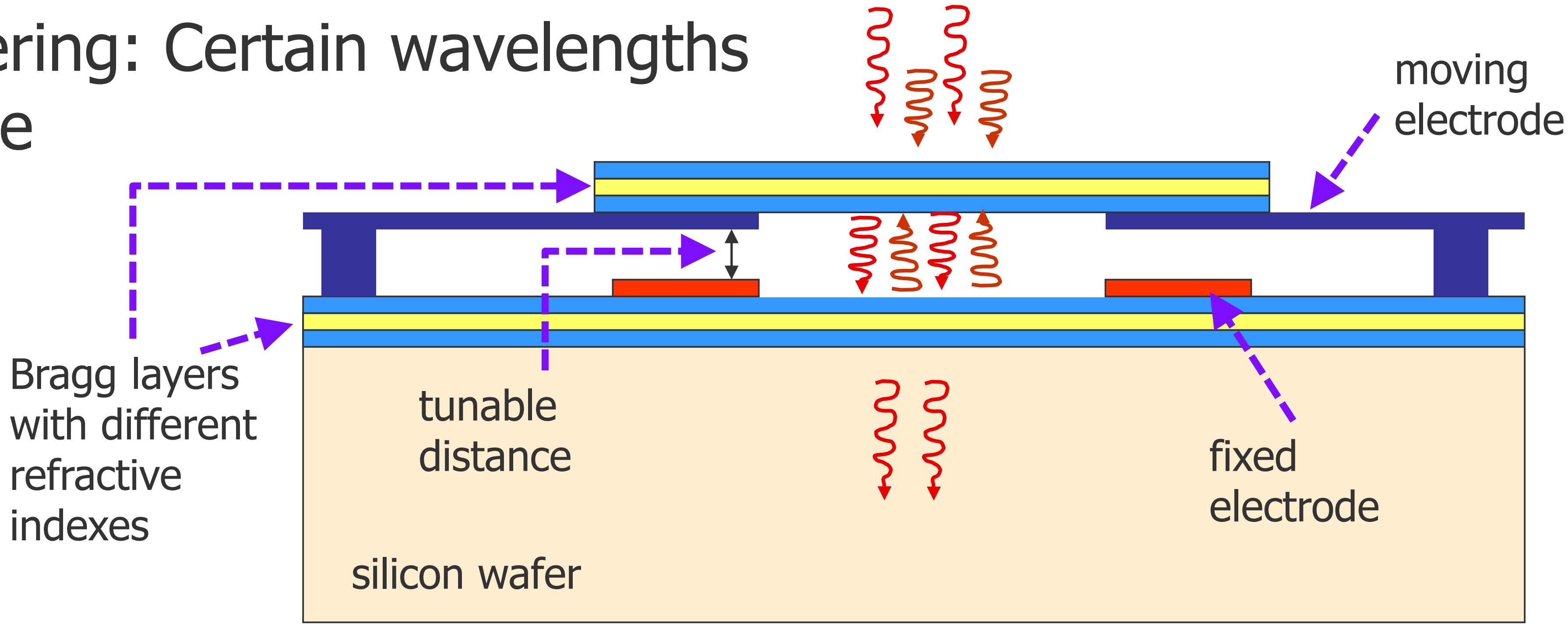
- Process and Mask Design changes to Improve Yield
- Sensitivity-What parameters need to be controlled?
- Design Centering- Variation Tolerant designs
- Design Optimization used to generate layout that is most tolerant



DEMO

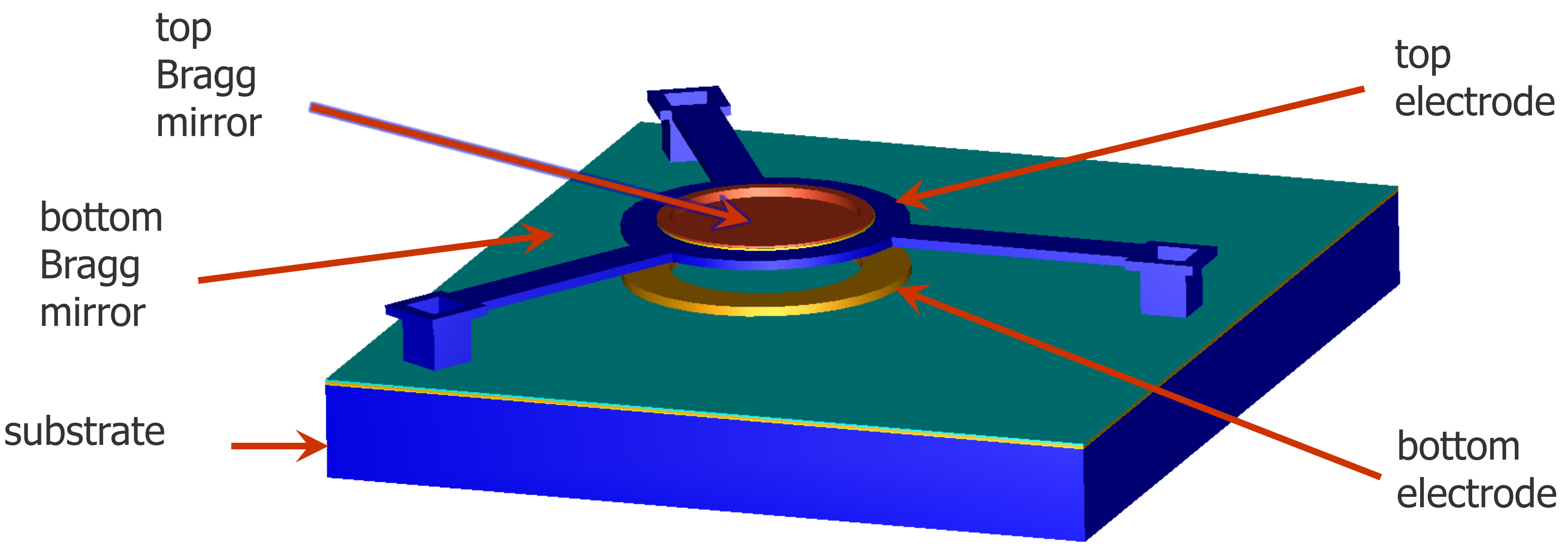
Tunable Filter for WDM Applications

- Tunable filtering:
  - The distance between two mirrors determines the range of frequencies that are filtered out
  - The distance between two mirrors is controlled by electrostatic actuation
- Wavelength filtering: Certain wavelengths are removed due to interference



Tunable Filter 3D Design

- Top electrode: metal ring suspended on three support arms
- Bottom electrode: polysilicon ring
- Top/bottom mirrors: layers of polysilicon, oxide, and nitride



IC TOOL FLOW

Design Flow

- Analog
- Digital
- Mixed-Signal

Analog Verification Manager:
Tanner Designer

Schematic Capture:
S-Edit

Design Entry:
ModelSim / Questa

Analog Simulation:
T-Spice, Eldo, Eldo RF, AFS

Behavioral Simulation:
ModelSim / Questa

Mixed Signal Analysis:
T-Spice AMS

Block Layout:
L-Edit, Interactive DRC, SDL

Synthesis:
Oasys AMS

Physical Verification:
Calibre DRC, LVS, PEX, PERC

Place and Route:
Nitro AMS

Post-Layout Simulation:
T-Spice, Eldo, Eldo RF, AFS

Functional Verification:
Optimus AMS / Formal Pro

Chip Assembly and Functional Verification:
L-Edit, SDL Router, Calibre, T-Spice, Eldo, AFS, ModelSim / Questa

Industry Initiatives

OpenAccess

IPL Interoperable PDK Libraries NOW.COM

Foundry PDKs

tsmc

X-FAB X-FAB SEMICONDUCTOR FOUNDRIES

VIS

TOWERJAZZ

UMC

ams

GLOBALFOUNDRIES

Dongbu HiTek Semiconductor Business

ON Semiconductor

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