

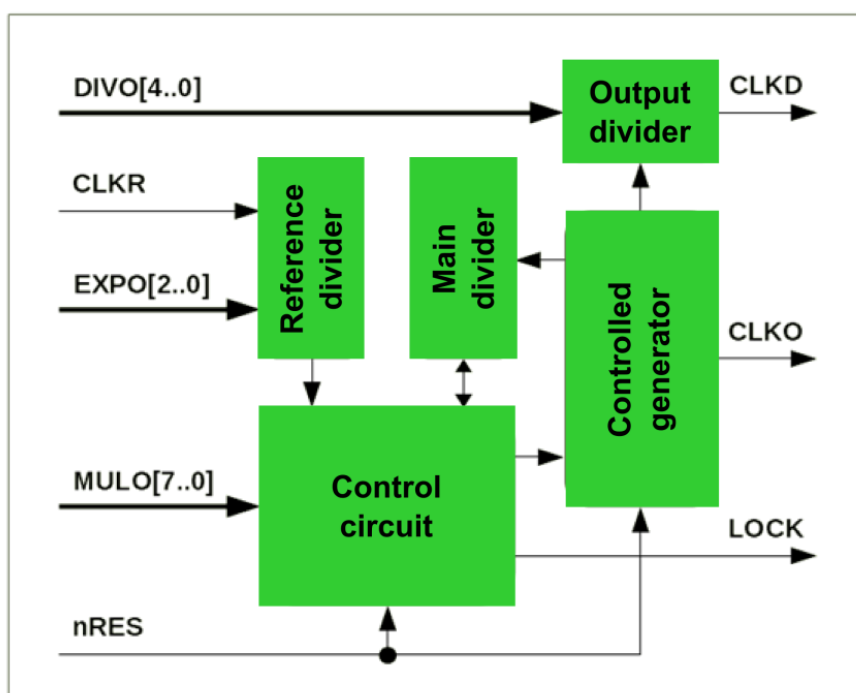
FULLY DIGITAL GLITCH FREE PLL

KEY FEATURES

- Ideal as a clock generator for digital design
- Excellent frequency jitter performance
- Ultra-low area fully digital PLL design
- Patented glitch free frequency adjustment
- Fine frequency precision with fractional divider
- Low implementation charges due to predictable digital design

DESCRIPTION

A programmable fully digital PLL (FDPLL) designed to lock to an incoming clock source and produce an output clock. It is ideal as a clock generator for digital designs, but not intended for analog blocks like ADC/DAC or SERDES clocking. This digital PLL has ultra-low area and low implementation charges due to predictable digital design.



In the capture mode PLL provides periodic signal on *CLKO* output with period equal to *CLKR* inputs period multiplied by *MULO:EXPO* value. Where *MULO:EXPO* is a denormalized floating-point number, *MULO* is an 8-bit mantissa, *EXPO* is a 3-bit exponent. Multiplication coefficient is calculated as follows: the *EXPO* exponent code [2..0] is interpreted as integer from 0 to 7, which determines the position of the binary point inside the *MULO* mantissa [7..0]. *EXPO* numerical value is the number of the *MULO* digit, followed by a binary dot dividing *MULO* into integer and fractional parts (the size of the fractional part). That is, for *EXPO* = 0, the fractional part is absent, and the entire integer part is in *MULO* [7..0]. For *EXPO* = 7, the integer part is in *MULO* [7], fractional in *MULO* [6..0]. In addition to the main output of the generator, the module has an auxiliary output *CLKD*, the frequency of which is obtained by dividing the main frequency by a factor of 2^{*DIVO} [4..0].

PLL CHARACTERISTICS

Parameter	Unit	Min	Typ	Max	Comment
CLKR reference frequency	MHz	0.8		1000	
CLKO output frequency range	MHz	200		2000	
CLKD output frequency	MHz	3.125		1000	
CLKO jitter	%		1		CLKO=600 MHz
				2	CLKO=1000 MHz
CLKO output duty cycle	%	45	50	55	
Power consumption	mW		5		CLKO=1000 MHz
Operational voltage	V	0.8	0.9	1.0	Digital only
Total area	mm ²		0.012		
Operational temperature	°C	0	70	85	

PIN LIST

Signal	Direction	Comment
nRES	input	Asynchronous reset input (Active Low)
CLKR	input	Reference frequency input
MULO[7..0]	input	Multiplication factor mantissa input
EXPO[2..0]	input	Multiplication factor exponent input
DIVO[4..0]	input	Post-divider factor input
CLKO	output	Basic frequency output
CLKD	output	Post-divider output
LOCK	output	Capture indication output