ЦИФ·МГУ

ACCESSIBLE DIGITAL TECHNOLOGY

FULLY DIGITAL GLITCH FREE PLL

DATASHEET

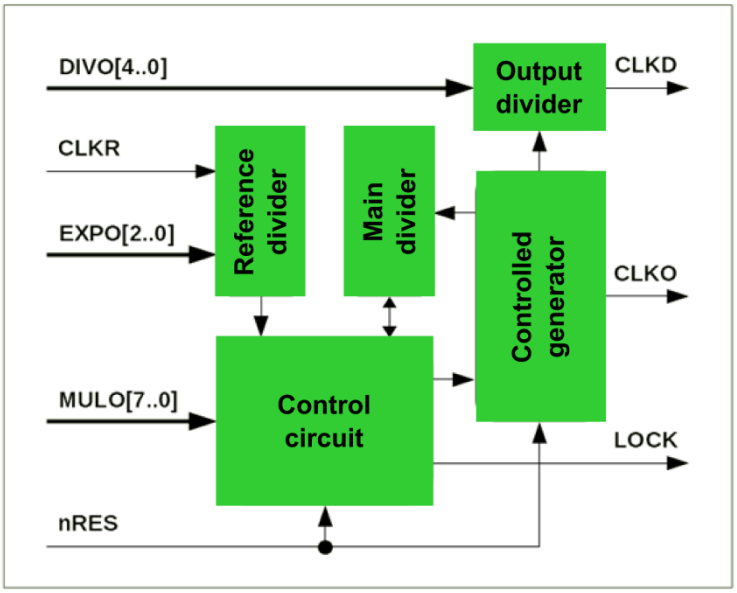
KEY FEATURES

- ∴ Ideal as a clock generator for digital design
- ∴ Excellent frequency jitter performance
- ∴ Ultra-low area fully digital PLL design
- ∴ Patented glitch free frequency adjustment
- ∴ Fine frequency precision with fractional divider
- ∴ Low implementation charges due to predictable digital design
- ∴ Available for all modern TSMC processes

HPC+ 28 nm **16FFC 16 nm** **N7+ 7 nm**

DESCRIPTION

A programmable fully digital PLL (FDPLL) designed to lock to an incoming clock source and produce an output clock. It is ideal as a clock generator for digital designs, but not intended for analog blocks like ADC/DAC or SERDES clocking. This digital PLL has ultra-low area and low implementation charges due to predictable digital design.



In the capture mode PLL provides periodic signal on CLKO output with period equal to CLKR inputs period multiplied by MULO:EXPO value. Where MULO: EXPO is a denormalized floating-point number, MULO is an 8-bit mantissa, EXPO is a 3-bit exponent. Multiplication coefficient is calculated as follows: the EXPO exponent code [2..0] is interpreted as integer from 0 to 7, which determines the position of the binary point inside the MULO mantissa [7..0]. EXPO numerical value is the number of the MULO digit, followed by a binary dot dividing MULO into integer and fractional parts (the size of the fractional part). That is, for EXPO = 0, the fractional part is absent, and the entire integer part is in MULO [7..0]. For EXPO = 7, the integer part is in MULO [7], fractional in MULO [6..0]. In addition to the main output of the generator, the module has an auxiliary output CLKD, the frequency of which is obtained by dividing the main frequency by a factor of 2*DIVO [4..0].

PLL CHARACTERISTICS *

Parameter	Unit	Min	Typ	Max	Comment
Reference frequency	MHz	1	10	2000	
VCO frequency	MHz	200		2000	
Auxiliary frequency	MHz			1000	
Period jitter	%		< 2		CLKO=1000 MHz
Power	mW			6,6	CLKO=1000 MHz
Operational voltage	V	0,8	0,9	1,0	Digital only
Total area	mm^2		0,01		
Operational temp	^oC	0	85	125	
Duty cycle	%	49	50	51	

* all data for TSMC HPC+ 28 nm

PIN LIST

Signal	Direction	Comment
nRES	input	Asynchronous Reset (Active Low)
CLKR	input	Reference frequency
MULO[7..0]	input	Mantissa of the multiplication coefficient
EXPO[2..0]	input	The exponent of the multiplication factor
DIVO[4..0]	input	Post-divider ratio
CLKO	output	The main frequency
CLKD	output	Auxiliary frequency after the divider
LOCK	output	Capture indication (Active High)